Cleaning Process Development and Optimization in the Surface Mount Assembly Line of Power Modules

by

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Submitted to the Department of Mechanical Engineering in Partial Fulfillment of the Requirements for the Degree of

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Abstract

The cleaning process in the surface mount assembly line of power modules had been found to insufficiently remove solder flux residue from printed circuit board (PCB) assemblies after the process of reflow soldering. This thesis details the development of an optimized cleaning process that effectively removes solder flux residue from PCB assemblies. The first stage of this study involves the experimental validation of root cause of process ineffectiveness. A novel visual inspection based grading scale is developed to quantify the amount of residue present. Using the grading scale optimal process parameters were identified and studied. The study finds that power modules are most effectively cleaned in a saponifier based cleaning solution using ultrasonic agitation. Power modules are completely cleaned when washed in an ultrasonic bath at 60°C for 7 minutes, in a saponifier based cleaning solution that is 5% concentration by volume.

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1. Introduction

This thesis is a result of a project carried out by a research team at the electronics power module manufacturing facility of Vicor Corporation. The application of the manufactured power module lies in the fields of computing, data processing, communications and controls; where the demand is for high product efficiency and reliability. The research team comprising of P Jain [1], N. Rajendran [2] and the author developed an efficient process to remove solder flux residue from printed circuit boards (PCB) after the process of reflow soldering. The study comprised of the root cause analysis of process inefficiency, process development & optimization and manufacturing system analysis. In this thesis, the focus is on the selection and optimization of a cleaning process which consistently removes solder flux residue from PCB's, thus eliminating related product failures.

1.1 Company Background

Vicor Corporation headquartered in Andover, MA is a market-leading provider of electronic power system solutions for the highly specialized electronics industry. The company designs and manufactures modular power components which have applications in various fields such as computing, communications, industrial control, industrial testing and medical and defense electronics. The company manufactures three types of products— Bricks, VI-Chips and Picor components. Bricks and VI-Chips are specialized D.C.-D.C. and A.C.-D.C. power convertors

and filters and include power regulators, current multipliers and bus convertors, whereas the Picor range includes high density power conversion circuit components. In this work, however, the focus is on the manufacture and quality improvement of VI-Chips.

1.1.1 Product Information and Description

VI Chip refers to the name given to the latest series of DC-DC converters released by Vicor which have higher power density, higher efficiency, improved transient responsiveness, lower noise levels and lower costs than the previous series of DC-DC converters. DC-DC converters are an integral part of many electronic and electrical applications and are used whenever there is a need to either step-up (also referred to as 'boost') or step-down (also referred to as 'buck') the input voltages in order to deliver an output voltage. A typical example could be observed in a car were different electrical appliances like headlights, radio, etc. require different input voltages and hence would need a DC- DC converter to convert the input voltage from the car battery to meet the different voltage requirements. This DC-DC conversion can be achieved through the VI – chipset which includes different modules like PRM (Pre-Regulator Module), VTM (Voltage Transformer Module), BCM (Bus Converter Module), etc. Evidently, each of these modules has different product architectures. But they can be still produced on the same production line.

The PRM can be predominantly associated with the voltage regulation work i.e. it delivers a highly regulated voltage from an unregulated input source. Though PRM can be used just as a power regulator, it is usually used in conjunction with the VTM which uses the regulated voltage from the PRM and transforms it according to the demand. Thus a PRM – VTM combination essentially serves as a regulated DC – DC converter. BCM module is a supplementary module which is a fixed DC – DC voltage transformer that can be used along with the regular PRM – VTM combination and usually used to provide intermediate voltages. This modular approach of having three or more different modules (PRM, VTM and BCM) for achieving the function of a

DC – DC converter is result of the 'Factorized Product Architecture (FPA)' philosophy introduced and followed by Vicor instead of the regular 'Centralized Product Architecture (CPA)' adopted by the rest of the industry.

1.2 Overview of Thesis

This thesis is a result of collaborative research work carried out by P. Jain [1], N. Rajendran [2] and the author from January through August 2011. The research team set out to first jointly study the manufacturing system and its constituent assemblies. This was followed by an in-depth research in the physics of the cleaning process and of the DI water based cleaning system installed in the facility. In this thesis, Chapter 2 explains these two stages by describing the manufacturing processes and the essential background concepts. Chapter 3 focuses on the formulation of the problem being tackled and sheds light on the specific details of the inefficient cleaning of solder flux residue. Following the problem statement, Chapter 4 presents a brief summary of industrial and academic research carried out in related fields. At this stage the thesis breaks off to elaborate on the individual work done by the author in selecting the best cleaning process and optimizing it. Chapter 5 explains the basis, methodology and testing procedures while Chapter 6 present experimental results and related discussions. Chapter 8 presents a summary of the work performed along with recommendations and possible future areas to be worked on.

2. Overview of Manufacturing Process

This chapter presents an overview of the manufacturing process followed in the production of VI-Chips at Vicor's facility in Andover, MA. The process flow includes the surface mount technology (SMT) process for attaching and soldering of components. This chapter also discusses in detail the post-SMT PCB cleaning, its necessity and the methods available for cleaning of boards.

2.1 VI Chip Manufacturing Process Flow

VI Chips are essentially power modules with surface mount devices (SMD) such as field effect transistors (FET), both in multi-wire lead-frame package (MLP) as well as ball grid array (BGA) forms, chip capacitors etc. Other parts on the chips include transformer core and J-leads. The primary step in the manufacture of VI Chips is the SMT process on the printed circuit boards. After surface mount of components, the boards undergo a cleaning process remove solder flux residues. The subsequent steps are transformer core attach, electrical testing, underfill, molding, marking and PCB dicing, J-lead attach and final testing. The flowchart in Figure 2.1 shows the different steps, with the main steps being briefly described in this section.

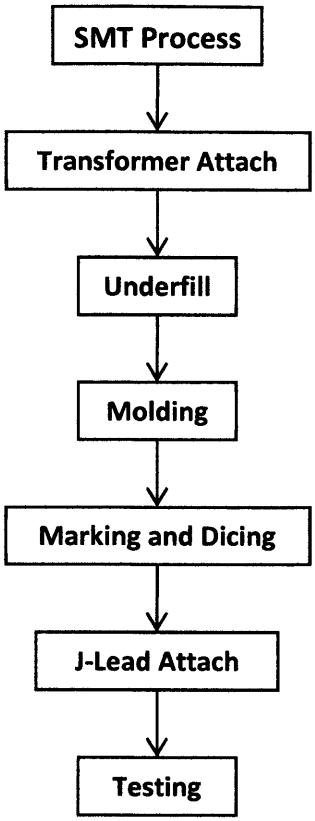


Figure 2-1 Flowchart of VI-Chip manufacturing process

2.1.1 Surface Mount Technology Process

The SMT process is a modern method used to construct electronic circuits in which components are directly positioned and mounted on the PCB. It involves a series of steps in which solder paste is directly applied onto the PCB and then components are mounted and the boards reflowed in a reflow oven to effect the soldering. The flowchart in Figure 2.2 shows the SMT process followed at Vicor.

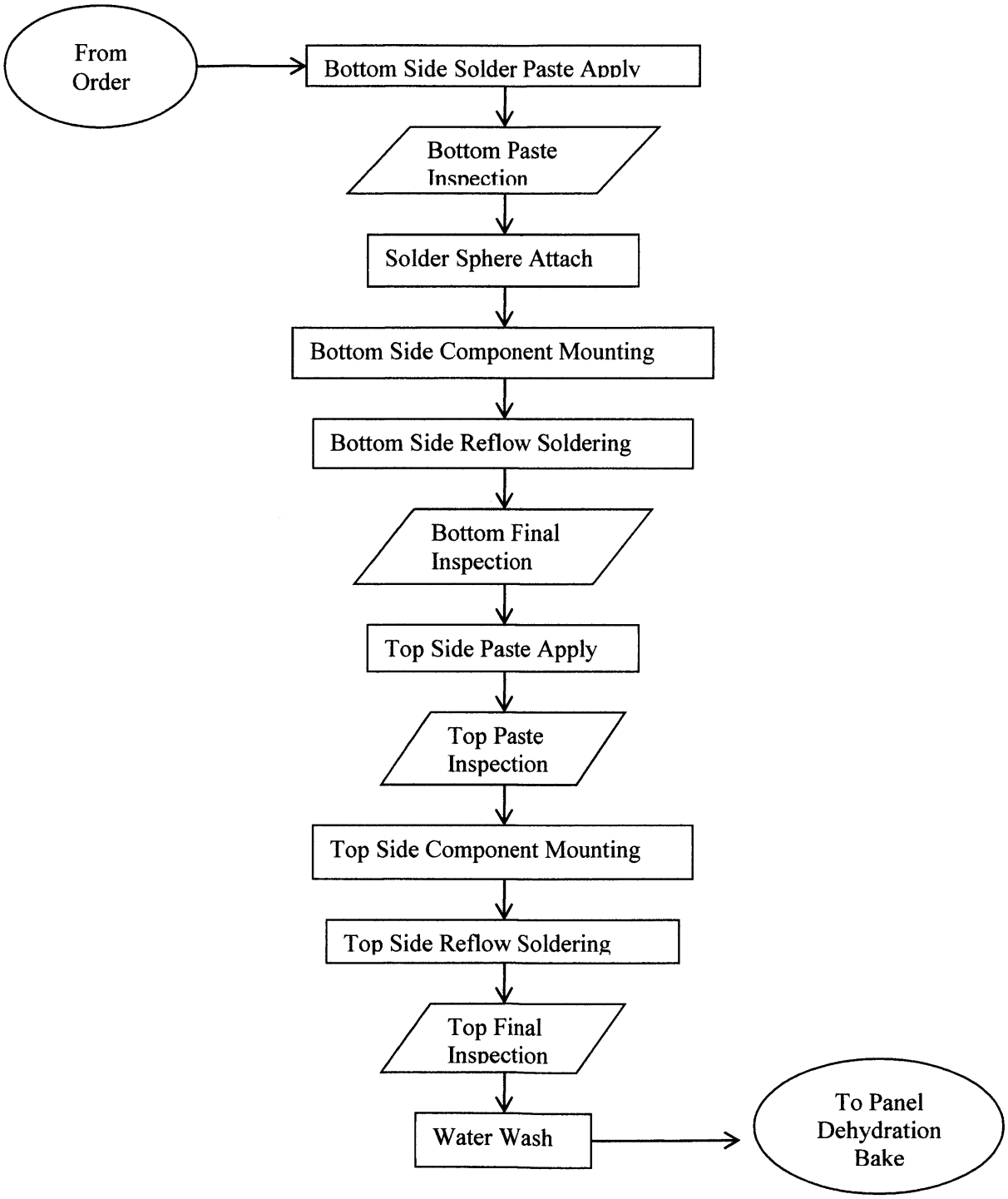


Figure 2-2 Surface mount technology process flow

2.1.1.1 Screen Printing

The first step in SMT is screen printing, which involves the use of a stencil with apertures to allow application of solder paste on the PCB only at required positions, with a squeegee applying the paste over the stencil, thus effecting transfer onto the PCB. The solder paste contains the solder alloy and flux. The current paste being used at Vicor is "*Indium 3.2 HF*" which contains 88.5% solder alloy and 11.5% flux by weight. The metallic part is a lead-free alloy of 96.5% tin, 3% silver and 0.5% copper, commonly known as SAC 305. The flux is an ORH0 type flux as per the J-STD-004 (IPC-TM-650) standards, which indicates an organic, halide-free flux that forms flux residue which is water-soluble. The flux is used mainly to:

- prevent oxidation of the solder alloy during reflow,
- act as a cleaning agent at the solder-component interface, and,
- provide the necessary tack for the components to stay at their locations till soldering occurs.

2.1.1.2 Solder Ball Attach

This process involves placing spheres of solder alloy, known as solder balls, at certain locations on the PCB. The solder balls are small, having a diameter of approximately 0.5 mm. The solder balls are used only on the bottom side of the PCB were a ball grid aray forms the J-lead attachment points.

2.1.1.3 Component Mounting

In this step, SMD components from a reel are mounted on the solder paste locations on the board. The components are placed precisely at their locations by the machine heads which remove the components from the reel and place them over their designated positions using fiduciary markers on the board sensed by the mounting machine.

2.1.1.4 Reflow

After component mounting, the next step is the soldering process. This is done by making the PCB go through a reflow oven. The reflow line has different temperature zones were maximum temperatures exceed 260°F (≈127°C). The high temperature partially melts the solder alloy contained in the solder paste, making it come in direct contact with the component leads. As the temperature reduces, the solder alloy begins to solidify, thus effecting the soldering. The recent growth in use of lead-free solder pastes due to environmental regulations have led to higher reflow temperatures, which cause flux cleaning problems. It may also be noted that in the manufacture of VI-Chips, the bottom side of the PCB goes through reflow twice – once for the bottom side and once for the top side. Post-reflow, the PCB is cleaned with deionized (DI) water to remove any flux residues.

2.1.2 Transformer Core Attach

After SMT, the next step is attaching the transformer core at the center of each module on the PCB. This core may be made of ferrite or other magnetic materials and plays the crucial role of stepping up or down the voltage. The attach process involves using an epoxy as glue for the core, placing the core on the epoxy, and then curing the epoxy to secure the core.

2.1.3 Underfill

Due to a difference in the thermal expansion properties of the components and the PCB substrate, there exists a risk of adding thermal strain on the solder joints of the components during any thermal cycle, which may cause joint failure. Underfill is the process of adding a locking resin between the components and the PCB substrate so that the components are fixed in place. This causes the thermal stress to act on the whole Underfill area, thereby relieving the solder joints of the strain. The resin used is generally an epoxy material.

2.1.4 Molding

Molding is the process of introducing a molding material such as a thermoplastic or resin over the PCB to package the components. During the process, the fluid molding material enters all empty spaces on the PCB, packing all the components in place. Molding can be done by compression molding, injection molding or transfer molding. The molding process is preceded by a dehydration bake and plasma etching for better mold compound adhesion.

2.1.5 PCB Marking and Dicing

After molding, the PCB is marked using a laser and then diced into individual VI-Chips using a saw. Subsequently, the individual chips are cleaned by first spraying DI water and isopropyl alcohol (IPA) and then cleaning using a brush. The cleaning is done to remove any contaminants or oxides which may prevent proper J-lead adhesion.

2.1.6 J-lead Attach

In this step, J-leads are attached onto the BGA points on the bottom of the VI-Chips. J-leads are specialized leads used to provide an interface between the VI-Chip and the external circuit. This is the last step in manufacturing.

2.1.7 Final Testing

After the VI Chips are made, the final step is the testing and quality checks. At this stage electrical tests such as high potential test are performed. Thermal tests are also performed to test for extremely high and extremely low temperature performance.

2.2 Post-SMT Cleaning

In Section 2.1.1, the process of PCB cleaning after SMT has been briefly mentioned. This section explains the cleaning process in detail, including why cleaning is done, cleaning methods and existing standards on cleaning.

2.2.1 PCB Cleaning

PCB cleaning is the process of removing solder flux residues from the PCB after the SMT process. The flux present in the solder paste reacts with the metal oxide during the reflow process and prevents further oxidation of the solder metal. The by-product of this reaction is the solder flux residue which gets trapped beneath components and near the undersides of solder balls. During the cleaning process, this residue is flushed out and dissolved by an aqueous (DI water) or semi-aqueous (DI water with chemicals) solvent using external agitation.

Cleanliness can be defined using many different tests. Tests are mainly of two types– visual and chemical-electrical. Visual tests include removing components and visually observing the presence of flux residues, while the chemical-electrical tests measure chemical and/or electrical properties to determine cleanliness. Cleanliness standards and testing have been described in subsequent sections.

2.2.2 Why Cleaning

The solder flux residue, which is trapped between the components and the PCB substrate and near the undersides of solder balls, is electrically conductive as it is made up of ions. As PCBs and modules are subjected to an external electric field, which in many cases involves relatively large potential drops, the diffusing flux residue particles get excited by the momentum transfer of conducting electrons in the circuit. This leads to the particles getting displaced from their positions. A problem may arise when these particles cause bridging between two parts of a circuit, ultimately leading to a short circuit. This phenomenon is called electro migration.

Another form of short-circuiting may be observed when the flux residue forms a bridge over a component. Shorting over components may also lead to component fracture by inducing a differential stress between the component and the surroundings.

Another possible effect of flux residue presence is the improper adhesion of the molding compound and J-leads. For proper adhesion to take place, the surface of the PCB and BGA areas must be free of contaminants such as flux residue. Due to these problems, effective cleaning of solder flux residue becomes imperative.

2.2.3 Factors Involved in Cleaning

A number of factors influence the cleaning process of PCBs and can be divided into two major types. One of the main factors is the choice of solder paste. The solder paste may have specific properties which may affect cleaning process. These properties could be physical properties of the flux residue such as viscosity, water solubility etc., chemical properties such as reactivity and corrosiveness and electrical properties such as conductivity. Another major factor is the reflow temperature. With the advent of lead-free soldering, the temperature required for effective soldering has increased, leading to changes in properties of the flux residue. One important factor is the amount of gap present between the component and the PCB substrate, called standoff. Lower standoffs lead to less effective cleaning.

The other set of factors include solvent properties, process temperature, type of external agitation, and exposure time. Solvent properties include use of only DI water or DI water with chemicals. Temperature influences cleaning by altering the surface tension of the solvent, altering the solubility and/or by activating the chemical present in the solvent. External agitation forces the solvent into the areas where the flux residue is trapped, thereby improving cleaning performance. Time is also an important factor as it defines the duration for which the cleaning action occurs.

All the above factors when combined effectively can produce good cleaning efficiency. The choice of factors depends on the requirements for cleaning the PCBs. The challenge is to carefully select and optimize the values in order to achieve the best possible cleaning.

2.2.4 Cleaning Methods

The semiconductor and allied industries have in the recent past been able to come up with many alternate methods of cleaning with each method suited to a particular type of product architecture. These different cleaning methods could be classified based on the nature of their primary approach towards cleaning as either physical agitation or chemical action based methods.

2.2.4.1 Agitation Methods

The three main methods which fall under this category are detailed below:

a) Centrifugal Cleaning

This method takes advantage of the agitation induced by the centrifugal force in a liquid medium which could range from just plain DI water to chemical solutions containing surfactants or solvents. The PCBs are usually held inside this medium and are subject to the centrifugal action during three major cycles namely wash, rinse and dry cycles though the addition of a fourth cycle namely the pre-wash cycle cannot be ruled out. Evidently enough, this method is a batch process with process times averaging around 20 minutes and the temperatures are usually above the room temperature varying between 55°C and 70°C across the different cycles.

b) In –line Cleaning

In-line method of cleaning is a relatively new development which uses water or a chemical solution sprayed at a pressure through custom designed nozzles over the PCBs which continuously move across a line through the machine. Recent advancements made in nozzle

technologies by certain companies have resulted in further improvement of cleaning efficiency. Though the throughput rates, the physical agitation levels and hence the cleaning efficiencies in an in-line machine are seemingly higher especially when compared to the centrifugal washing machine, these machines are characterized by high cost as well as high wastage of DI water or chemical solution.

c) Ultrasonic Cleaning

This method uses the physical agitation made possible by the superimposition of the ultrasonic waves originating from a transducer, inside a liquid medium. The superimposed waves produce a cavitation effect where vacuum bubbles are constantly formed and undergo implosion. This agitation effect in a chemical solution medium has been found to give encouraging results, although the time taken could be long as one only side of the board could be cleaned at any given time. This method has also been known to have mildly destructive effects on the minute surface mount devices.

2.2.4.2 Chemical Methods

This category includes methods were the chemical action is predominantly responsible for cleaning. Many commercial companies have introduced different chemical solutions that achieve the purpose. Most of these chemical solutions are either surfactants or solvents that tend to drastically reduce the surface tension of DI water so that it is able to reach the minute pockets and the remotely accessible areas of the product.

2.3 Process Control and Testing

As with any other manufacturing process, the cleaning process too has its own set of process control tests which could be used for monitoring the process. These tests vary in the time taken for testing, costs involved and also in the requirement of manual supervision.

2.3.1 Process Control Tests

Though both ionic and non-ionic contaminants are found on the surface of the board, the ionic contaminants are of particular interest since they have the potential to cause electro-migration and similar other problems. The following are some of the more commonly used tests:

2.3.1.1 Ionic Contamination Test

The ionic contamination test also known as the Resistivity of the Solvent Extract (ROSE) test, is predominantly used in most of the industries thanks to its simplicity as well as its versatility. In this test, the boards are immersed in DI water for about 5 minutes and later the DI water is tested for contamination which is measured in terms of milligrams of sodium chloride (NaCl) per square inch. But this method also suffers from serious deficiencies as it can measure only ionic contamination and does not reveal the source of the contamination. In many of the cases, the contaminants present in inaccessible areas go undetected in this test.

2.3.1.2 Ion Chromatography

Ion chromatography is a more sophisticated and time consuming test where the boards are kept in clean ion-free bags and then placed in a bath containing 75% alcohol and 25% water and maintained at 80°C for at least an hour. This test color codes the different types of ions present on a board and most importantly indicates the source of these ions.

2.3.1.3 Surface Insulation Resistance (SIR) Test

The SIR Test measures the contamination by conducting an electrical test across a solution in which the board has been soaked and then measuring the current which gives an idea of the resistivity of the solution which in turn can be directly correlated to the level of contamination.

2.3.1.4 Fourier Transform Infra-red (FTIR) Spectroscopy

This is another optical inspection test which scans the board with infra-red light and uses the resultant image to analyze for contamination. This image is then compared with industry standards to identify the contaminants. This test is most generally used in the industry to identify the organic contaminants.

2.3.1.5 Visual Inspection

Visual inspection gives the most detailed result among all the different tests but it is a very laborious process and requires manual supervision. At a magnification of 50X, it is possible to observe the flux residues on a VI-Chip. The visual inspection is preferred especially when there is a need to know the location and the distribution of the flux residues.

2.3.2 Inadequacy of Current Testing Methodology

At present, the ionic contamination test is regularly carried out on the products coming out of the washing process and the results of the test are plotted on control charts which are then used for monitoring the process. On reviewing the test results and the control charts, it was observed that the ionic contamination levels do not cross specification limits, as described by industry standards. This occurs even though there have been flux residues observed on the board surface and underneath components. The main reason for this is that the ionic contamination test actually measures the resistivity of the solution based on the amount of residue washed and dissolved, rather than the amount of residue on the board. Thus, the test results in a number of false negatives for flux residue presence.

3. Problem Statement

The SMT line forms the first section of the production assembly line in the manufacturing facility, Figure 3-1. All products mentioned in Chapter 1 are manufactured in the facility and are chiefly comprised of surface mount devices. The SMT line can be divided into the sub-sections of solder paste printing, solder ball placement, components mounting, reflow soldering and the water wash cycle. All sub-sections are followed by inspection stages which are either automated vision system based inspection or manual inspection as in the post-reflow inspection station.

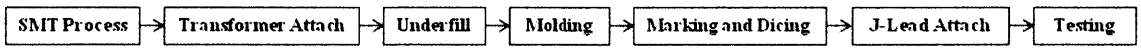


Figure 3-1 Process flow chart

Since the product has a double sided architecture it has components on either side of the PCB board hence the process of solder paste printing, component mounting and reflow soldering is carried out twice; first on the bottom side of the PCB board and then on the top side of the board. Furthermore, the bottom mounting process also includes a stage where solder balls are placed for a BGA.

The assembly line beings with the screen printing of solder paste on the bottom part of the PCB board using a stencil based screen printing process; the solder printing is inspected using an in built in vision system. This is followed by the placement of solder balls on the required regions such as the BGA for J-Lead attach and for external interface. Once the solder paste and

solder balls are positioned, the components on the bottom side are mounted on their respective specific regions. The placed components are fixed to the PCB board via solder joints which are formed when the PCB boards are passed through a reflow-soldering oven. The reflow process involves processing the boards through a temperature profile that melts the solder material from the paste to form strong solder joints.

This process is repeated for the top surface as well but without the solder ball process as the architecture does not require solder balls on the top surface. After the reflow process the boards which were part of a single piece flow on an assembly belt are placed in cartridge. These cartridges carry 10 boards at a time and are carried over to the visual inspection station. At the visual inspection station boards are randomly sampled and inspected for improper component placement or solder joint faults.

The last stage of the SMT line is the PCB board cleaning station. The station consists of two centrifuge based water wash equipment which have a capacity of cleaning two cartridges at a time i.e. 20 boards, using DI water

3.1 Problem Description

The PCB board cleaning station or the water wash station comes after the second reflow process and the manual inspection stage. The DI water based centrifugal washing machine is responsible of removing all flux residue and other contaminants from the surface of the boards and the modules contained in them. However as illustrated in Figures 3-2 and 3-3, over a period of time it was found that repeated quality tests showed the presence of flux residue on the products. With the objective of maximizing product efficiency and reducing product failure rates, this occurrence was termed as highly avoidable and had to be investigated and corrected.

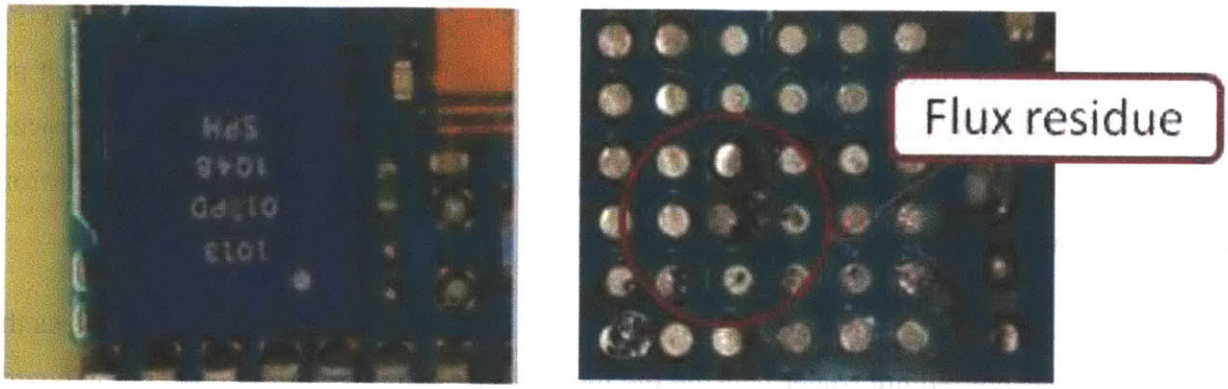


Figure 3-2 Presence of flux residue under a BGA-FET

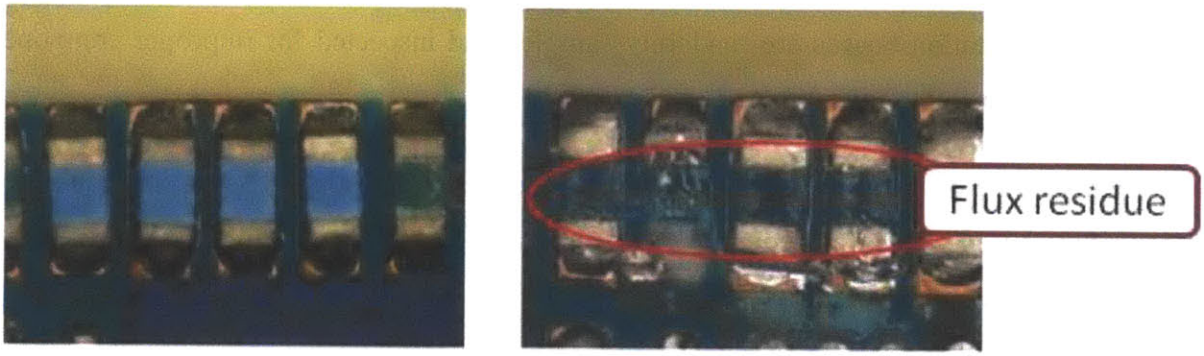


Figure 3-3 Presence of flux residue under chip capacitor array

As per process design, the testing of all components is carried out after the last stage of packaging that is the J-lead mounting cycle. The test cycle inspects all components for their electrical integrity. When components are found faulty, they are sent to the quality department for quality analysis (QA). The QA cycle involves a wide range of tests of which destructive testing is the main procedure, where the surface mounted components are pried out off the PCB board and then inspected for integrity of solder joints, solder shorting, presence of flux residue etc.

Over a period of time since the introduction of the particular product nearly all packages were found positive for flux residue presence. Flux reside was observed on the board and also

under surface mount components. It should be known that as the test cycle is at the end of the assembly line, the cause of fault cannot be cornered onto a particular process and only possible causes can be discerned. It was the management's viewpoint that although it cannot be definitely proved that products were failing due to the presence of flux residue, the issue was stark enough to be worked on.

3.1.1 Areas of Residue Incidence on PCB

The inspection or products revealed the presence of flux residue in nearly all inspected products on the board near and around solder joints and under certain components.

a) Near and Around Solder Joints

Once the mold compound was cut off the products white colored flux residue was observed on the surface of the PCB board. As shown in Figure 3.4, the residue appeared as a random scattering of white colored particles in clear areas or as rings surrounding solder balls. Further inspection proved them to be water-soluble flux residue that was left behind due to inefficient cleaning.

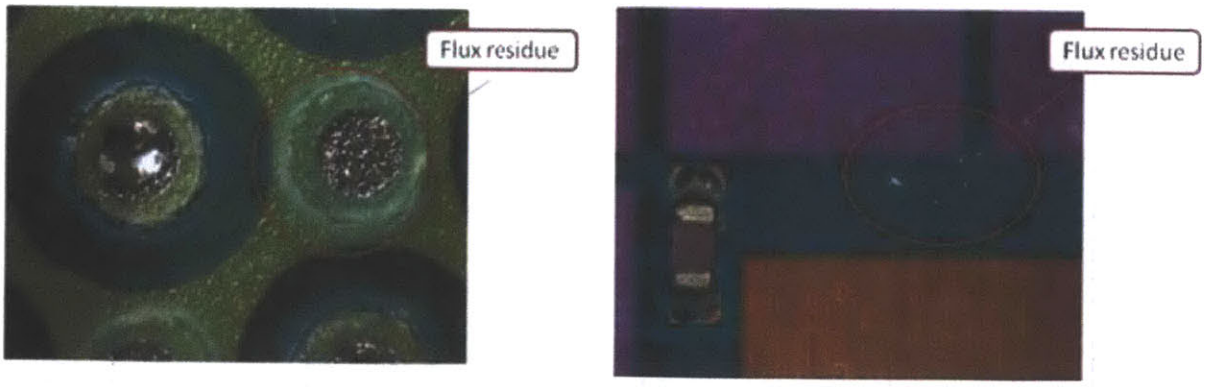


Figure 3-4 Flux residue around BGA's and on board

b) Under "low standoff" components

The term "standoff" refers to the distance between the bottom surface of surface mount components and the top surface of the PCB board. As the products being manufactured are highly compact the components such as 1201 chip capacitors and MLP-FET have standoffs lower than $50\mu m$. Figure 3-5 illustrates the definition of a "standoff", it shows a MLP-FET whose distance between the bottom surface of the controller and the surface of the PCB board is $50\mu m$. In reality this distance is just about the thickness of the copper laminate that forms the electrical network i.e. the components are virtually placed flush with the PCB surface with only the copper laminate forming a very small gap. The difficult to remove solder flux residue from these in small gaps is shown in Figure 3-6, an image of the underside a MLP-FET which has significant flux residue along the leads.

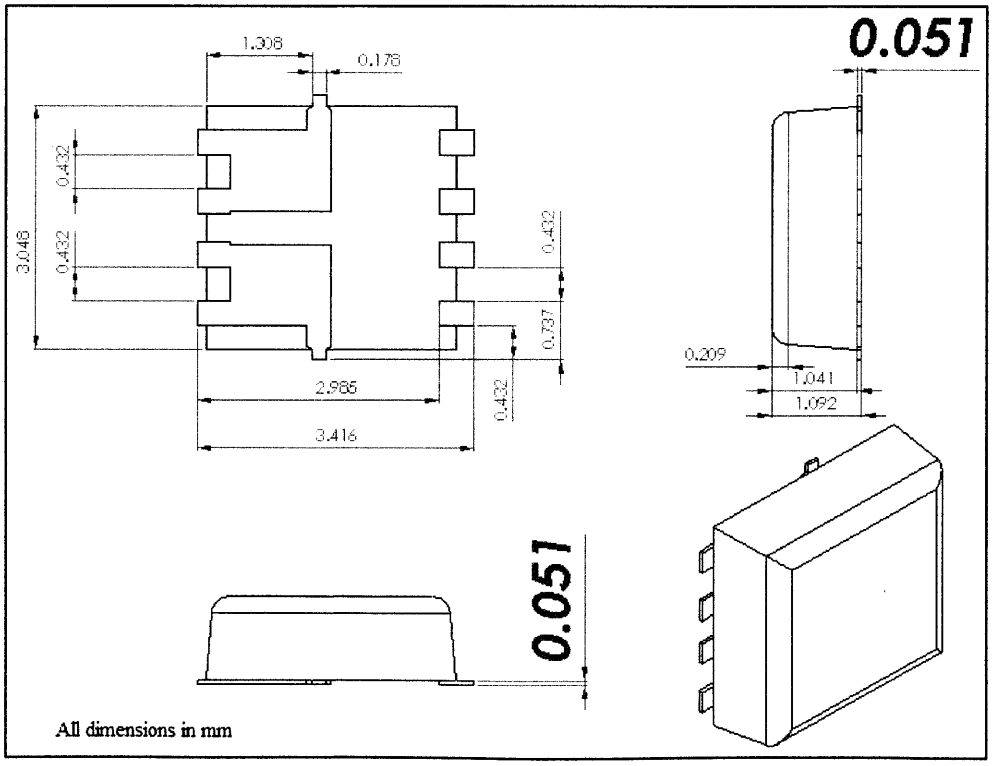


Figure 3-5 Diagrammatic description of "Standoff" in a MLP-FET

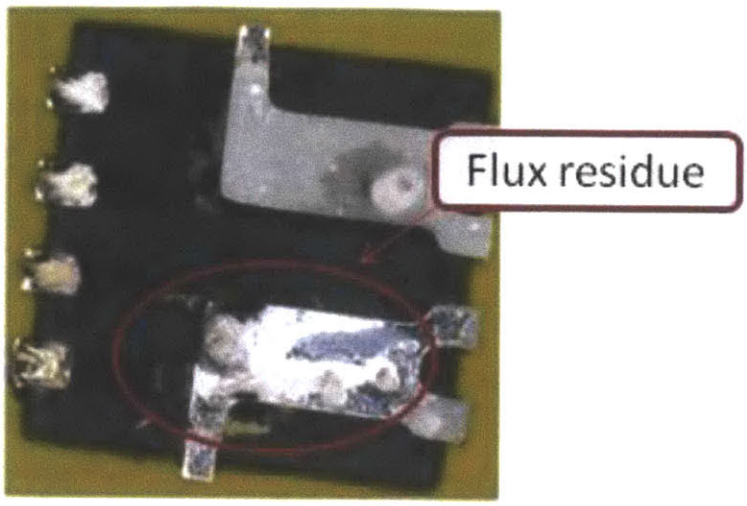


Figure 3-6 Flux reside on bottom surface of MLP-FET

Similarly, quality assurance inspections revealed that nearly all components with low standoffs contained solder flux residue. As illustrated in Figures 3-7 and 3-8, components such as QMOS, chip capacitors showed presence of flux residue when they were pried off the PCB board.

Figure 3-7 Flux reside on QMOS footprint

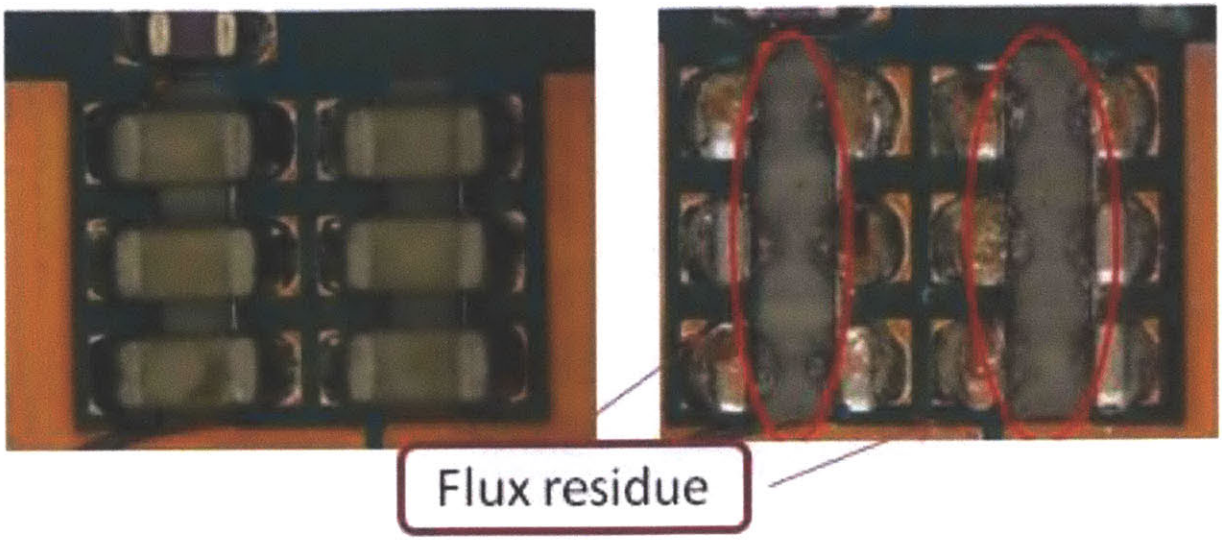


Figure 3-8 Flux reside on chip capacitor array footprint

3.1.2 Effects of Flux Residue

The presence of flux residue on the surface of the PCB board and under component adversely affects the product inefficiency as highlighted in Section 2.2.2.

3.1.2.1 Electromigration

Electromigration is an electrochemical process where metal on an insulating material, in a humid environment and under an applied electric field, leaves its initial location in ionic form and re-deposits somewhere else[15]. Such migration may reduce isolation gaps and ultimately lead to an electrical short circuit. Electromigration may affect the reliability of flip-chip solder joints as the eutectic solder used is a two-phase alloy, so its electromigration behavior is different from that in aluminum or copper interconnects.

The presence of flux residue on the modules could provide a path for development of a potential [8]. The process starts if a thin continuous film of water along with residue forms an

oppositely charged electrode. Positive metal ions are formed at the positively biased electrode anode, and migrate toward the negatively charged cathode. Over time, these ions accumulate as metallic dendrites, reducing the spacing between the electrodes, and eventually creating a metal bridge. The formed metal bridge would cause solder shorting when potential is applied thus inhibiting the proper functioning of the module.

3.1.2.2 Poor Mold Compound Adhesion

In the manufacturing process once all the components are mounted on to the PCB board the products move to the molding cycle. In this process the products with underfill under the components are molded to encapsulate the package. This process involves covering a molten material over the components which is then allowed to cool to forma hard cover to protect all the surface mount components. This process involves adhesion of the mold compound to the PCB board, for this to take place efficiently the PCB should be clean and free of any contaminants.

Furthermore the manufacturer is moving to replace the current molding process by a "molded underfill" process. This removes the underfill stage completely as the mold compound is used for both molding the product and also as the underfill material. As the mold compound has lesser surface tension than the conventional underfill material, the presence of flux residue and contaminants would make under filling much more difficult.

3.1.2.3 Improper J-Lead Attach

Similar to the issue of poor mold compound adhesion the attachment of J-Leads is severely affected by the presence of flux residue near and around the BGAs. The occurrence of flux such as the case illustrated in Figure 3-9 hinders proper soldering of the J-Lead to the BGA. The J-lead is attached to the BGA in the same way as all other components, it is first placed onto the BGA and then the unit is passed through a reflow process were the temperature profile fuses the J-Lead to the solder balls thus fixing it to the product.

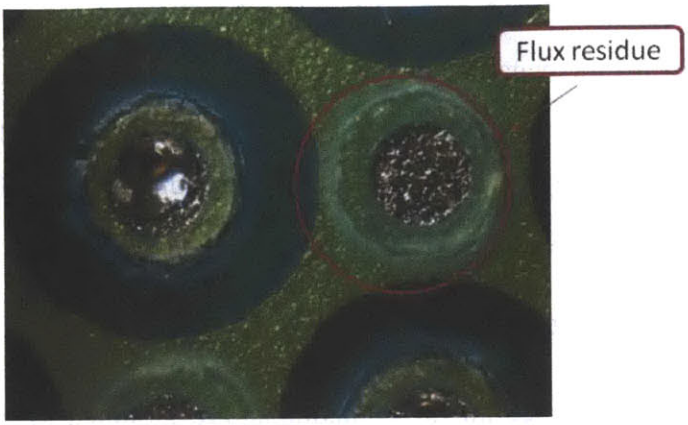


Figure 3-9 Flux reside around BGA older balls

Hence, if flux residue is present on the surface of the solder balls and also around its periphery the solder joints formed would be contaminated producing solder joints which lack the structural integrity desired.

3.2 Factors Involved

The centrifugal washing process removes solder flux residue from the PCB boards by either physically washing out flux residue or by chemically dissolving it. The principal factors that determine process efficiency are the process variables which contribute to the physical and chemical energy generated in the cleaning process which are agitation, chemical action, wash time and temperature of cleaning solution.

3.2.1 Agitation

The type and magnitude of agitation determines whether sufficient agitation is generated for the solvent to flow into low standoff region. This would firstly help to loosen the flux residue to

flush it out and secondly expose the flux residue to the solution which would simply dissolve it. In the current process, agitation is provided by the centrifugal action of the wash tank and also by two sets of nozzles. As the centrifuge rotates the DI water contained in it attains a state of turbulence, this enables DI water to flow into low standoff regions. The nozzles provide additional agitation by spraying DI water into low standoff regions to wash and rinse the PCB boards.

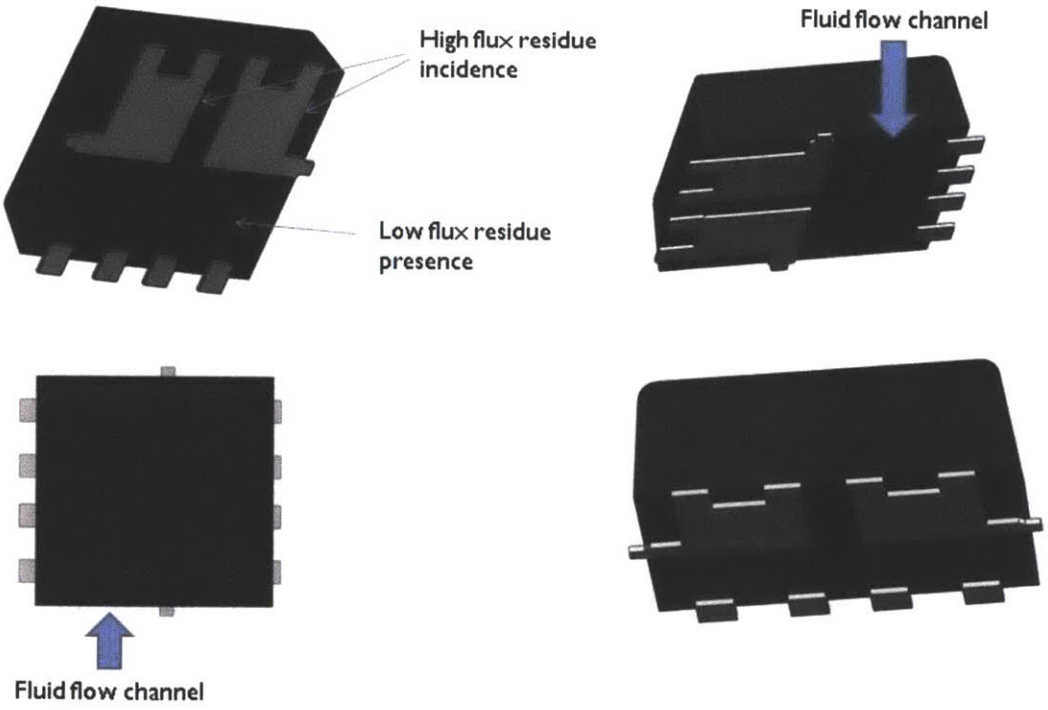


Figure 3-10 Illustration of fluid flow beneath MLP-FET

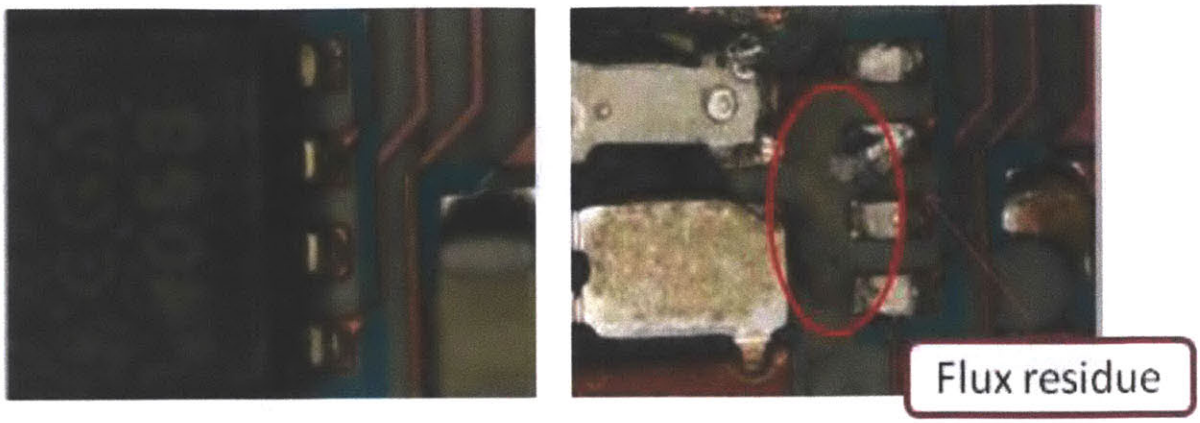


Figure 3-11 Presence of flux residue due to improper agitation and fluid flow

3.2.2 Chemical Action

The chemical characteristics of the solution determine how effectively the flux residue is dissolved. Solutions with saponifying agents act to reduce adhesion of solder flux residue to the PCB board; they reduce surface tension of cleaning medium for effective penetration into low standoff areas and then chemically acts on the residue and helps dissolve it. The current process does not use any form of saponifier and uses only DI water during the wash process because of the belief that with enough agitation, water would be able to access low standoff regions to dissolve flux residue. It is to be noted that as the flux residue is completely water soluble in nature, water is sufficient to dissolve it completely, and any other chemical agent assists only in reducing the surface tension to enable DI water to flow into low standoff regions.

3.2.3 Wash Time

Along with agitation and chemical property another important factor is the duration of the wash process. Higher wash times would provide more exposure time of the boards to DI water for loosening and dissolving of flux residue. As the agitation generated by a centrifuge is random,

longer wash times would allow for a much higher chance for the DI water to access low standoff regions.

3.2.4 Temperature

The fourth most important factor is the temperature of the washing solution. As water solubility increases with increase in temperature higher wash cycle temperatures would improve cleaning efficiency; as explained in Chapter 4 this phenomenon has been proven in past studies and experiments. Furthermore, in saponifier based cleaning increased temperature increases the chemical activity of the saponifier. Other benefits of higher temperature are improved solubility of residue and lower surface tension of water.

3.3 Project Objectives

In the Section 3.1 and 3.2, it was seen that effective removal of solder flux residue is vital for product manufacturability and reliability. Thus, it becomes imperative to develop a cleaning process which removes solder flux residue from products, while achieving maximum production speed and quality with minimum cost. To achieve these objectives the research team set out to tackle the problem by splitting it into the following parts:

- Identify the root cause of the flux residue problem through hypotheses formulation and experimental validation.
- Determine optimal process parameters to select and optimize most suitable cleaning process
- Perform manufacturing system analysis to monitor and study the effect of developed process on system efficiency.

This particular thesis deals chiefly with the second part with brief elaboration of the first and third parts. The work of Jain [1] explains in detail the root cause analysis of the problem, while Rajendran [2] illustrates on the findings of the developed manufacturing systems simulation model. In subsequent chapters, the selection and development of an optimized cleaning process has been discussed.

4. Literature Review

The importance of efficiently removing solder flux residue from components is well appreciated within the electronics manufacturing field [6]. With the increasing miniaturization of electronic assemblies, electronic products are moving to smaller size, higher density, higher speed and lower cost [5, 9]. Furthermore, in the mid 1990's environmental regulations resulted in the implementation of international standards such as RoHS and REACH [6] which pushed the electronics manufacturing industry towards halogen free and lead free soldering. As a result of such technological advancements and environmental regulations, designers and manufacturers are faced with the challenge to maintain acceptable standards of cleanliness.

The ability to remove flux residue after a soldering process from a electronic component is dependent of various factors of which product architecture and the solder flux used are the two most important[10]. The family of products studied in this work is comprised of surface mount technology components which are either chips scale packages (CSP's) or ball grid array BGA components. BGA components such as FET's have significantly higher standoff heights as compared to CSP's [12]; their standoff heights range from $457\mu m$ to 508 μm while CSP's could have standoff heights less than 50 μm. Research by Mearig and Goesrs [12] has shown that cleaning under BGA's is not a difficult process using semi-aqueous cleaning solutions; on the other hand the significantly smaller standoff heights of CSP's have found to be very difficult to be cleaned by numerous academic and industry studies [4, 5, 7, 8 and 10]. The standoff heights of CSP's were found to vary from component to component due to variation in manufacturing of their lead frames and the minimum standoff height was found to be 30.5 μm [7] . To tackle the

problem of cleaning components with low standoff heights the industry has strived to achieve the optimal combination of type of solder flux and the cleaning technique used to clean it.

After the implementation of environmental regulation the two major families of solder flux used are conventional lead free solder fluxes and no-clean solder fluxes. A majority of the industry leaders have adopted no-clean fluxes [5] due the non-requirement of a cleaning process which facilitates it to be used in complex product architectures [4]. However, it has been seen that in some cases even no-clean solders are cleaned to remove contaminants [7] and it produces process variations during component placement. The products researched in this study were manufactured using a water soluble lead free solder paste as prior experiments using no-clean solder fluxes had resulted in high assembly failure rates. The change in the composition in lead free solder pastes has had significant effects on the physical characteristics of the solder paste such as the melting point and the required reflow temperatures [4]. Due to higher reflow temperatures there is a high probability of a tin-salt formation along with increased bonding between the fluxes and the panel base. Hence, although lead free solder systems are environmentally desirable the cleaning of the flux residues is more difficult [10].

With the adoption of complex solder systems the utilization of appropriate cleaning process is critical. In seminal studies such as [7] & [15] in-line DI water cleaners were used however such cleaning systems are associated with significant capital costs and running costs. Lee in his studies [4, 6 and 10] has stated that mechanical agitation is an important factor in the cleaning process techniques such as spray-in-air, spray-under immersion, ultrasonic waves and centrifuge have been found to show consistently good results. The chemical concentration of the solvent used during the cleaning process has also been found to be a critical factor [10]. Semi-aqueous and aqueous solvents when used along with appropriate agitation techniques give good cleaning efficiencies. Lee also states that test procedures such as SIR, ionic contamination and ion chromatography have characteristics which make it suitable for a particular flux type and with each test having its advantages and disadvantages.

Prior to this work a study was carried out by the product manufacturers to optimize the DI water based centrifugal cleaning process that was used in the SMT assembly line [3]. The study found that cleaning water temperature, extended wash time, position of product in washing fixture and wait time after reflow did not change the amount of flux residue found on the product after cleaning. Consequently, the proven inefficient of the DI water based centrifugal cleaning process emphasizes the need for adopting a technique that is best suited to the architecture of the product being manufactured and the water soluble lead free solder flux being used. This literature illustrates the study that was carried out applying findings from literatures mention above to develop and optimize an efficient cleaning process.

5. Cleaning Process Development

The process of developing an optimal technique to remove solder flux residue required understanding of the root cause of the problem. To achieve this objective, the physics of the centrifugal washing process was studied. This involved studying the flux chemistry, agitation effects, chemical methods of cleaning and the dynamics of flow of the cleaning medium [1]. Based on study it was hypothesized that the repeated occurrence of solder flux residue after the centrifugal DI water wash process was due to the low standoff heights of the surface mounted components. The inability to remove flux residue from low standoff regions was due to three possible factors:

- Adhesion of solder flux residue on PCB Board and components, preventing physical flushing out of residue.
- Ineffective agitation generated by cleaning process to access low standoff regions, preventing chemical dissolution and physical flushing out of flux residue.
- Hindrance to the flow of cleaning solution due to component and product architecture issues.

In his work [1], Jain explains the basis of these hypotheses and how they would help decipher the root causes of the solder flux residue problem. In order to understand the root causes these hypotheses were tested for validity through a series of experiments.

5.1 Root Cause Hypothesis Validation

To understand the root cause of the problem a series of detailed experiment were carried out to test the validity of the developed hypotheses. The tests were designed to help identify the critical factors responsible for inefficient cleaning. To simulate the actual production process the experiments were designed to be carried out within the production cycle. The validation experiments were carried out by introducing a new process station between the final inspection and water wash cycle. As illustrated in Figure 5-1, this station named "Pre-Wash Test Cycle" allowed the ability to vary the factors explained in Section 5.1

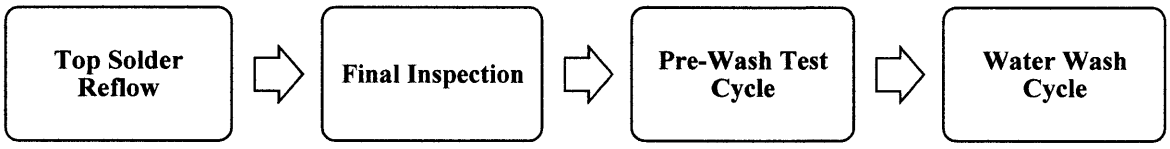


Figure 5-1 Hypotheses validation experiment process flow

5.1.1 Pre-Wash Test Cycle

To test the validity of the developed hypotheses and to find out the critical factors determining process efficiency, all process parameter were required to be varied. The water wash cycle was converted to a prewash and water wash cycle to study the change in cleaning efficiency with change in agitation, temperature, time and solution concentration. The pre-wash cycle effectively became the stage where the solder flux residue was acted upon either physically or chemically and the water-wash acted as more of a rinsing cycle to flush away the dissolved flux residue.

5.1.2 Design of Experiments

To test the validity of the formulated hypotheses the four primary process parameters were varied in the soak/ultrasonic process. The different process parameters are detailed in Table 5-1.

Table 5-1 DOE process parameters

Process Parameters	Factor Levels
Type of Agitation	Ultrasonic, Soak
Concentration of Cleaning Solution (conc. % by volume)	Deionized Water
	5,7.5, 10 & 12.5 Chemical B
	7.5 Chemical A
Process Time (minutes)	2 , 5 ,10, 20, 40, & 60
Cleaning Solution Temperature (°C)	60 , 70

The experiments were performed in the following two stages:

Stage 1: Hypotheses Test Experiment

In this stage all factor levels were varied to find out the effect of each process parameter on cleaning efficiency. To do this, a flexible DOE was developed (Appendix A) to understand the variation of each process parameter.

Stage 2: Water Wash Process Optimization and Test for repeatability

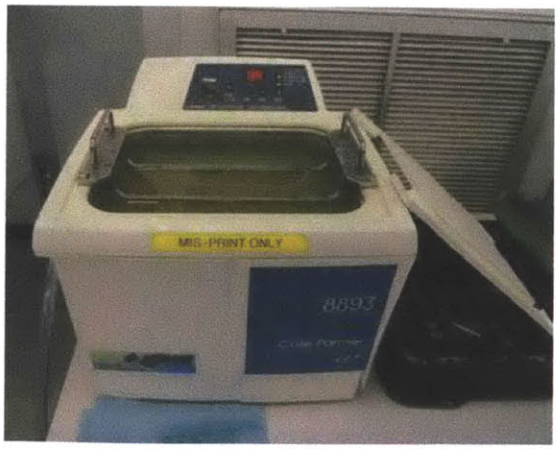
The centrifugal water wash cycle was retrofitted to allow introduction of Chemical B into the wash cycle. This formed the second stage of the experiment where cleaning efficiency of the water wash process was studied with variation in the concentration of the cleaning solution. Furthermore, this stage also involved repetition of important Stage 1 experiments to test for repeatability of test results as in Appendix A.

5.2 Experiment Methodology

The experiments were carried out by placing each individual PCB board in its designated cleaning recipe in a water bath and subjected to either ultrasonic agitation or plain soak without any external agitation. After the stipulated time, the boards were immediately processed through the 20 minute centrifugal water wash cycle followed by drying in a dry chamber. Once the boards were completely dry, they were subjected to inspection to determine the presence of flux residue in the sample.

5.2.1 Equipment and Test Board

The equipment used as the pre-wash test cycle was the "Cole-parmer 8893 ultrasonic cleaner" shown in Figure 5-2a. This particular cleaner had been used in the assembly line to clean misprinted PCB boards and was retrofitted to conduct the designed experiments. The equipment was chosen as it had a water bath with a 9.46 liters capacity which enabled the tested board to be immersed completely in the cleaning solution. Furthermore the equipment was capable of heating chemical solution up to 75^0 C, providing ultrasonic vibration with 42 kHz frequency and accurately monitoring experiments times.



Capacity		**9.46 Liters**
Tank dimensions	**Length**	**29.25 cm**
	Width	**24.30 cm**
	Height	**15.25 cm**
Frequency output		**42 kHz**

Figure 5-2a Cole-parmer ultrasonic cleaner

The power module "*V.I Chip- Full TV-36372*" shown in Figure 5-2b was selected as the test vehicle. Figure 5-3 shows the PCB boards that contain 16 of these power modules with surface mount components. This particular product was selected as the test vehicle as it provided an architecture that was highly dense with several components having critically low standoff of less than $50\mu m$. As it can be seen in Figure 5-3 the product architecture has dense surface mount components such as 1210 Chip Capacitors and MLP FET's on either side of the product.

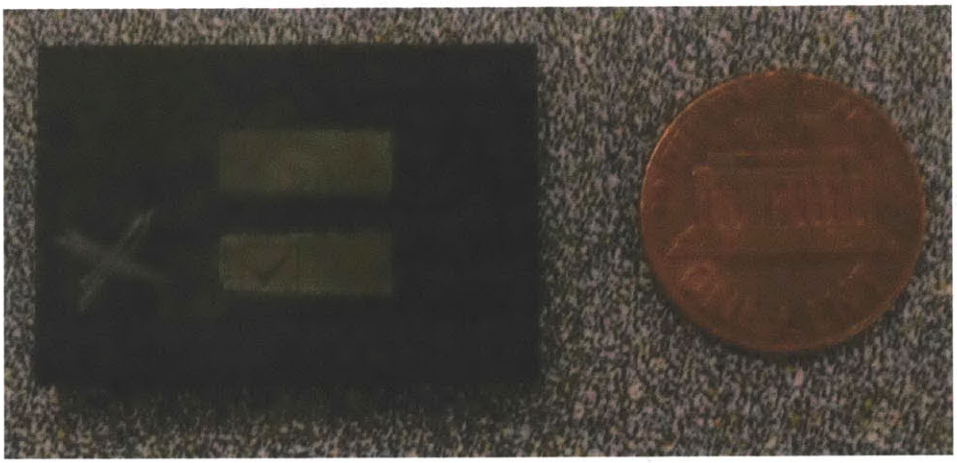


Figure 5-2b Test vehicle power module: V.I Chip -Full TV-36372

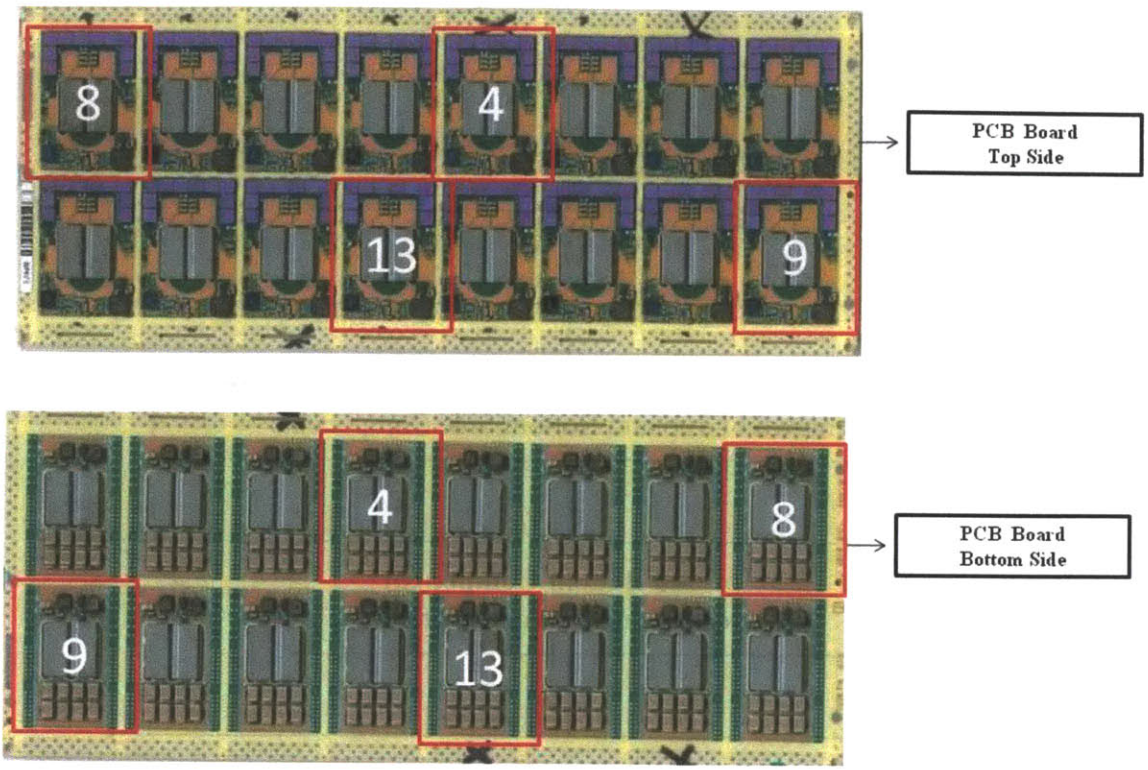


Figure 5-3 Experiment test board: V.I Chip-TV-36372

5.2.2 Inspection Methodology

The objective of inspection of the sample boards was to generate information of flux residue incidence. The sample boards, once water washed and dried were inspected in the Quality Assurance Laboratory in the production facility. Figure 5-4 below illustrates the flow chart of the inspection process implemented.

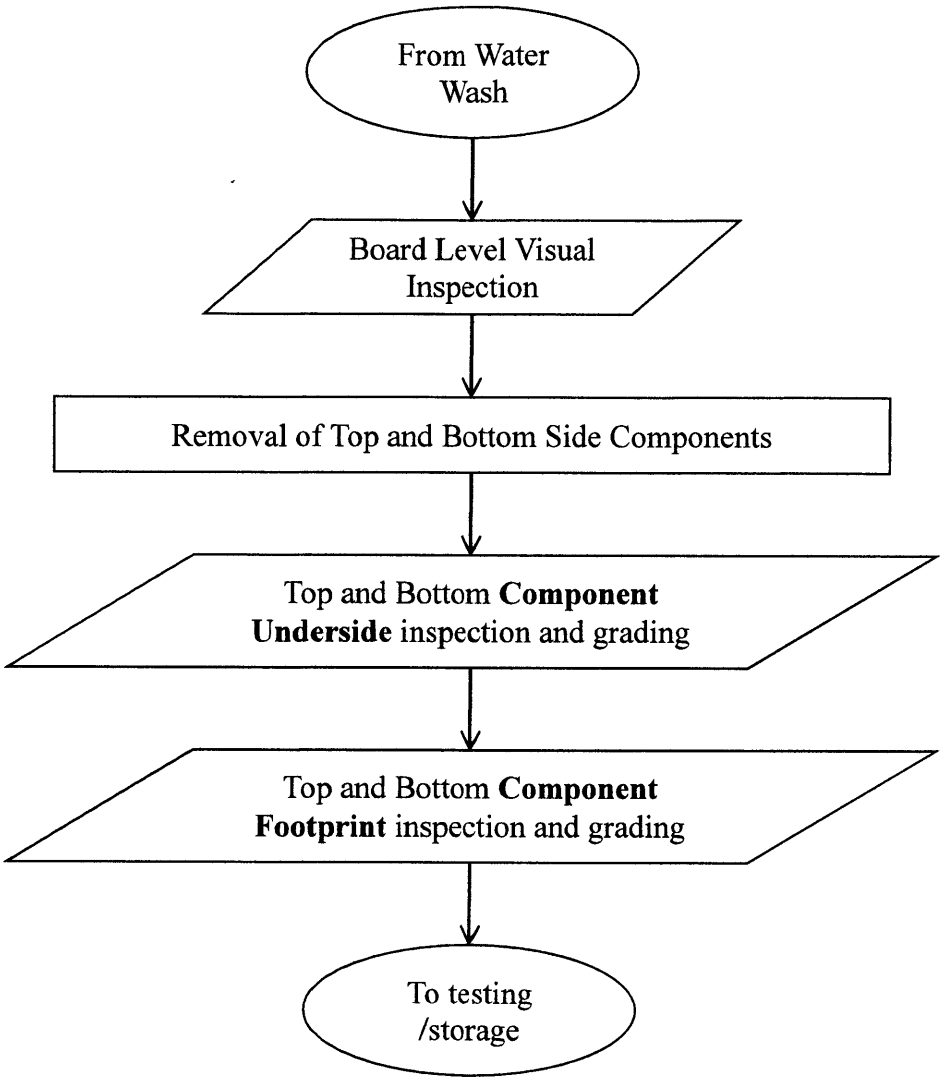
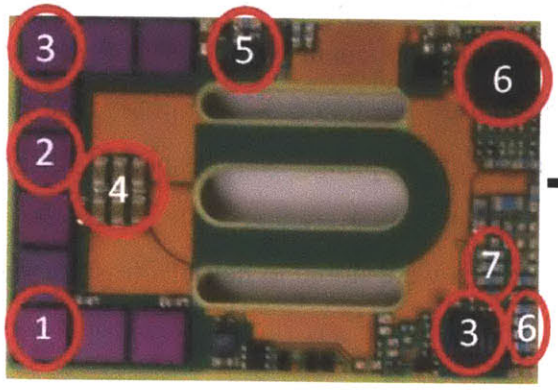


Figure 5-4 Inspection process flow chart

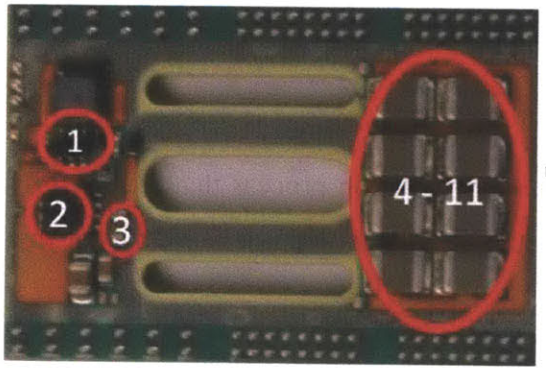
Stage 1: Board Level Visual Inspection and Component Removal

The first stage of inspection involved visual inspected for board level anomalies such as discoloration of copper pad, missing component, deformation and visible solder flux residue. Board inspection was followed by precise removal of components from the top and bottom side

using precision hammer and chisel. Module Numbers 4, 8, 9, and 13 in Figure 5-3 were inspected from each board. These boards were selected to provide an estimate of cleaning efficiency across the architecture of the PCB board. Modules numbered 4 and 9 were inspected as they were positioned in the middle of the center board and modules numbered 8 and 13 were selected as they were positioned on either end of the PCB board.



TOP SIDE	
Label #	Component
1,2,3	BGA FET
4	0603 Chip Capacitor
5,9	CSP-IC PRM2
6	MLP Controler
7,8	0402 Resistor



BOTTOM SIDE	
Label #	Component
1	Transducer
2	MLP FET
3	0603 Chip Capacitor
4:11	1210 Chip Capacitor

Figure 5-5 Inspected components on top and bottom side of power module

As illustrated in Figure 5-5 a total of 20 components were pried off each module making it a total of 80 components for inspection per board. On the top side 9 components such as BGA-FET, 0603 Chip Capacitors and MLP were studied as all of them possessed standoff in the rage of 50 μm to100μm. The BGA-FET was critical as the component was mounted on an array of

solder spheres where there was a high possibility of solder flux residue presence. On the bottom side 11 components were studied of which the MLP FET and the array of 1210 Chip Capacitors were most critical. Both of these components possessed variable standoffs of less than $50\mu m$.

Stage 2: Component Underside and Footprint Inspection

After the components were pried off, they were placed in glass slides and their undersides were inspected under a high resolution microscope. Each component was observed, imaged and then scored according to the scoring scale illustrated in the Section 5.2.3. Similarly, the PCB boards were inspected using a microscope; the "component footprints" were inspected for presence of solder flux residue and scored according to the developed grading scale. Once the inspection process was completed components and PCB boards were stored in non-electrostatic packages or sent for further testing if required.

5.2.3 Cleaning Efficiency Metric

It was found during the initial stages of the experimentation process that standard tests such as ion chromatography or surface insulation resistance (SIR) would not be viable for this particular study. This was due to their:

- Inability to detect change in the low amounts of solder flux residue in the products
- Inability to provide component and location specific data.

As a result a novel visual inspection based cleaning efficiency metric was developed to quantify the effectiveness of each experiment in removing flux residue from the PCB board. The developed metric detailed in Table 5-1 is a 0 to 5 scale, zero (0) indicates large amounts of flux residue and five (5) indicating no presence of flux residue.

Table 5-2 Cleaning efficiency metric description

Cleaning Efficiency Metric	
Score	**Description**
5	Completely Clean
4	Trace- Minute Amounts
3	Low flux residue incidence
2	Non-Uniform residue presence
1	Uniform residue presence
0	Large amounts of residue

The metric was used to quantify each component underside as well as component footprint on the board. Observation sheets such as ones show in Tables 5-3 & 5-4 were developed to allow systematic and exhaustive accounting of each component.

Table 5-3 Example of footprint observation data-sheet of Board A

Footprint Observation Data-sheet																					
Board No.	Module No.	Top Side Components									Bottom Side Components										
		1	2	3	4	5	6	7	8	9	1	2	3	4	5	6	7	8	9	10	11
A	4																		*3*		
	8				*3*			*3*					*2*								
	9									*4*						*5*					
	13			*3*											*2*						

Table 5-4 Example of component underside observation data-sheet of Board B

Underside Observation Data-sheet												
Board No.	Module No.	Bottom Side Components										
		1	2	3	4	5	6	7	8	9	10	11
B	4											
	8	*3*	*4*	*4*	*5*	*4*	*3*	*3*	*3*	*4*	*2*	*2*
	9											
	13											

With further examinations, there was a need to make the scoring metric more accurate and its description more accurate. The first stage was to understand the behaviors of solder flux residue and then form pictorial references for each phase. It was observed that for both inspection stages, certain components had distinct presence of solder flux residue thus a specific metric scale were developed for the following components:

Component Footprint Study:

- Top side 0603 Chip Capacitor (Component # 4)
- Bottom Side MLP-FET (Component #2)
- Bottom Side 1210 Chip Capacitor Array (Component #s 4-11)

Component Underside Study:

- Bottom Side MLP-FET (Component #2)
- Bottom Side 1210 Chip Capacitor Array (Component #s 4-11)

The component footprint metric scale is detailed in Appendix C while the component underside metric scale is detailed in Tables 5-5 and 5-6 and Figures 5-6 and 5-7.

Table 5-5 1210 Chip capacitor cleaning efficiency metric

Component Underside Cleaning Efficiency Metric : 1210 Chip Capacitor	
Cleaning Score	**Description**
5	Clean with no visible flux across surface.
4	Traces of white flux residue only near leg adjacent to copper pad
3	Significant flux residue near leg adjacent to copper pad and traces near other leg
2	Significant flux near both legs.
1	Uniform and non-granular smearing across surface.
0	Burnt it, hard yellowish layer across entire surface.

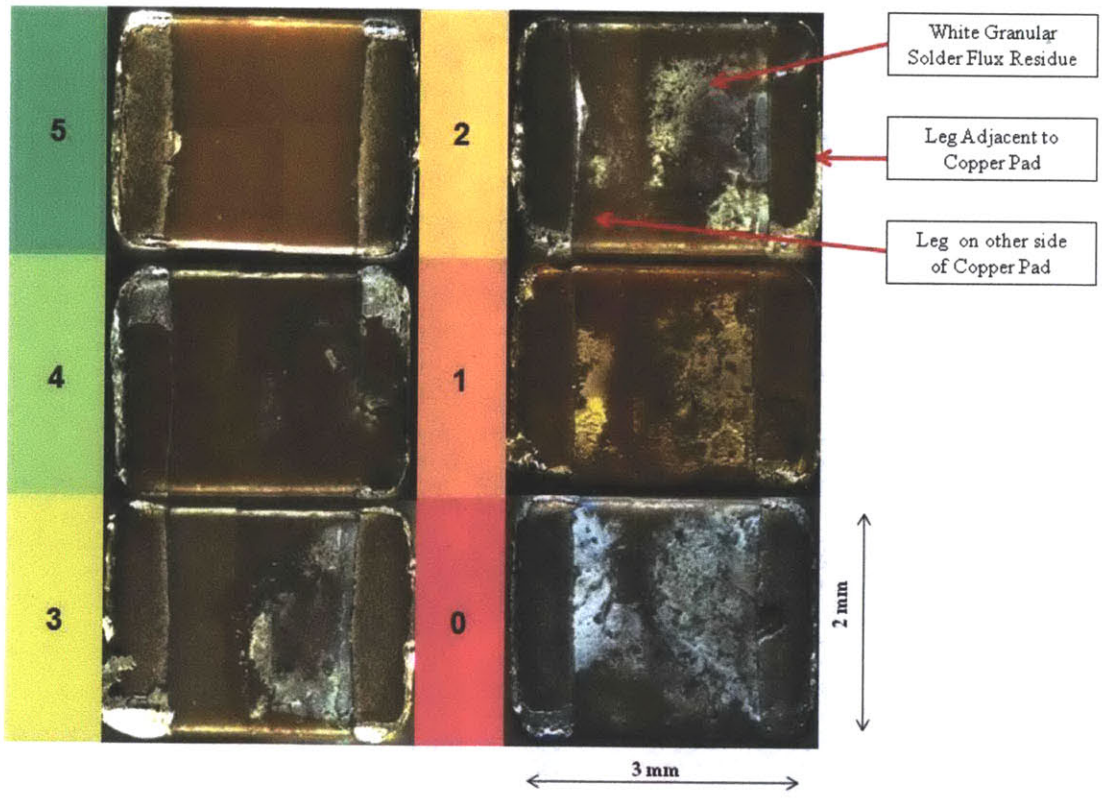


Figure 5-6 1210 Chip capacitor metric pictorial reference

Table 5-6 MLP FET cleaning efficiency metric

Component Underside Cleaning Efficiency Metric : MLP-FET	
Cleaning Score	**Description**
5	No visible flux on corners, middle channel and through channel.
4	Traces of flux residue in only in corners
3	Viable residue in corners and middle channel only
2	Significant flux residue in corners and middle channel with traces in through channel
1	White Granular and uniform flux residue across leads
0	Burnt in, crust like yellow flux residue across all sides of leads

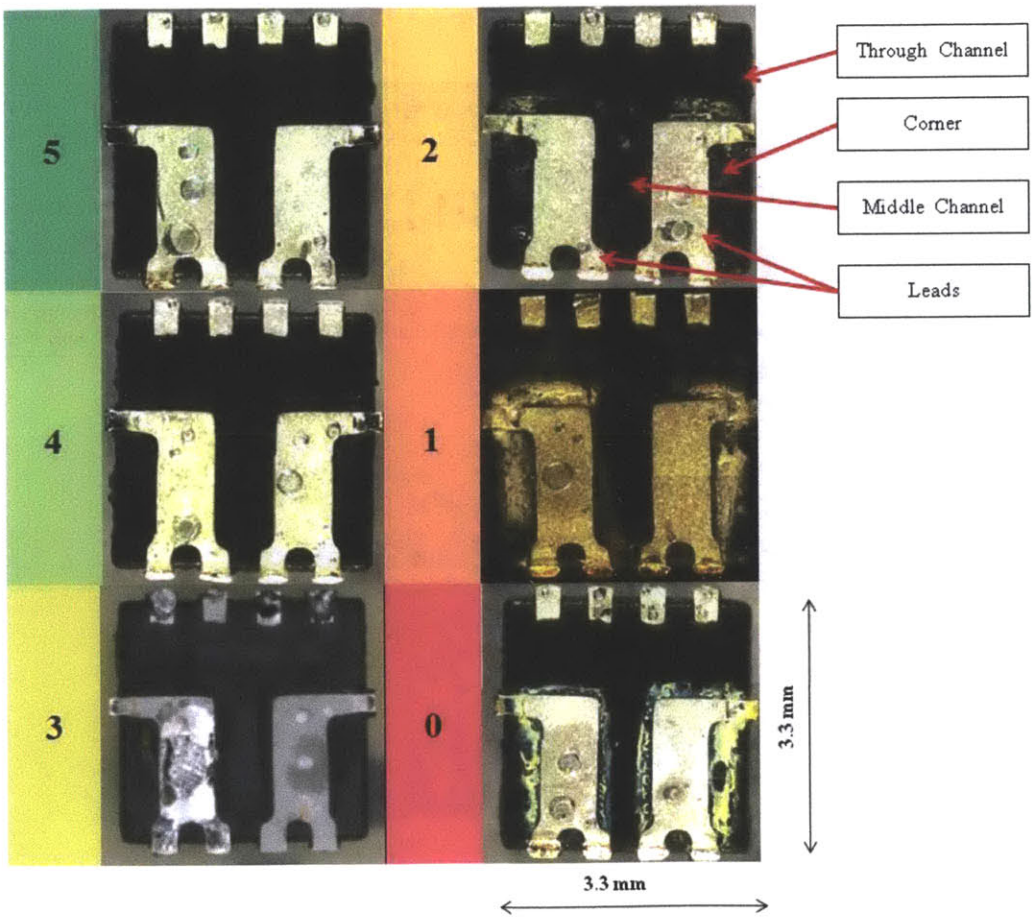


Figure 5-7 MLP-FET metric pictorial reference

5.2.4 Gage R&R Study

The novel cleaning efficiency metric developed in this work was a result of extenive inverstation and had not been applied before. As it was product specific and not gerneric, the variations in the obseverd data had to be studied to determine accuracy and applicability of the scoring metric. To enable this a gage R&R study was carried out to assess the amount of variation contributed by each source of measurement error, plus the contirbution of module to modue variability. Sources of the measurement error could be:

Repeatability: The variability from reperated measurements on the same module by by same inspector.

Reproducability: The variability when the same module is measured by differnet operators.

For accpetability of the metric, the difference between modules should have formed a large portion of the variability; and variablity from repeatability and reproduccibility should have very small. The study was carried out by the inspection of eight PCB boards by Jain[1] and the author. Measuremtns were made on all the components by two innspectors, thus giving a large enough data set to analzye the variability.

Table 5-7 Gage R&R study results: percentage contribution of variations

Source	Variance Component	% Contribution
Total Gage R&R	0.04	9.53
Repeatability	0.04	9.53
Reproducibility	0.00	0.00
Inspectors	0.00	0.00
Module - Module	0.42	90.47
Total Variation	0.47	100.00

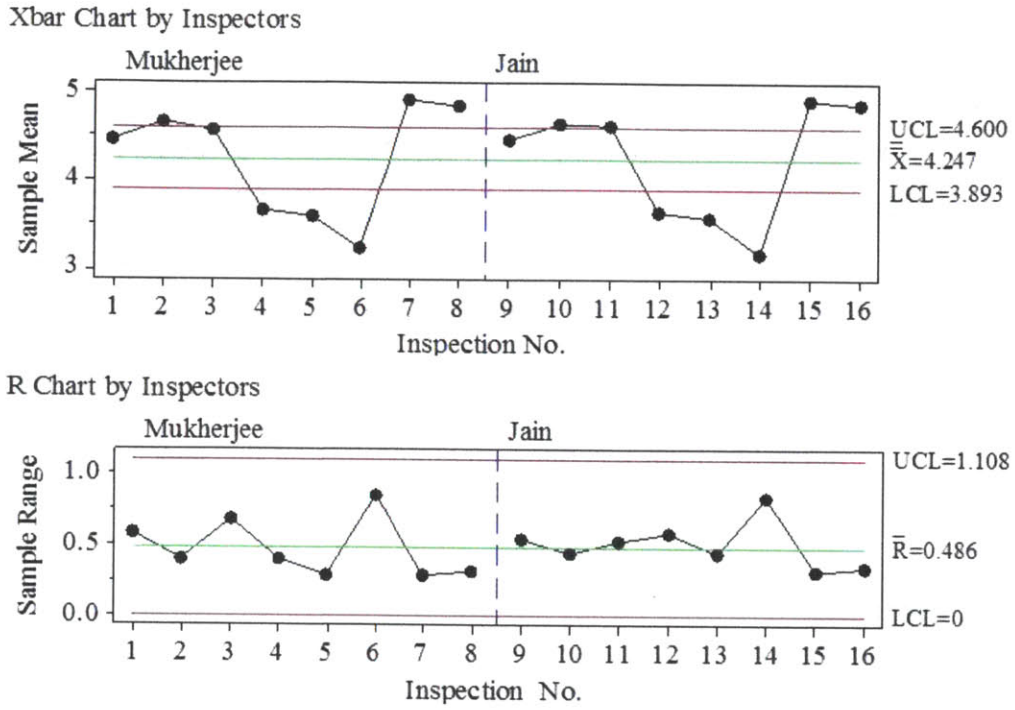


Figure 5-8 Gage R&R study control charts with study variation of 6 standard deviations

The results of the Gage R&R study (Appendix B) revealed that the developed metric was acceptable with minimal reproducibility error. Table 5-7 illustrates that 90.47% of the total variation was attributed to variations between different modules in a board and 9.53% was attributed to repeatability error i.e. error due to repeated inspection by the same observer. The contribution of inspector and reproducibility error was found to be negligible implying high levels of inspection accuracy across different inspectors. This finding was elaborated in the control charts shown in Figure5-8, where it can be seen that measurement taken by both inspectors was nearly identical. The control charts were drawn with a variation of six times the standard deviation which was 0.68, thus the Xbar chart also indicates the presence of significant error between separate modules.

5.3 Cleaning Process Selection and Optimization

The hypotheses validation experiments were designed to give information regarding the root-cause of cleaning process inefficiency and how each process parameter contributes to the removal of solder flux removal from low standoff components. On completion of the validation experiment the next step involved the analysis of the extensive experiment data to understand the system at work and select the best cleaning method. This process selection phase was followed by the optimization of the selected cleaning method with the objective of maximizing process efficiently and process rate while minimizing total cost of production.

5.3.1 Analysis of experiment data

The experimental methodology explained in Section 5.3 produced 20 data points per module and 80 data points per PCB board. The validation experiments were carried out across 38 test PCB boards, thus producing of around 3,000 data points. Furthermore, during inspection numerous images were taken as reference for further study. With the data-sheets shown in Tables 5-3 and 5-4, each of these data-points was accounted for in a systematic manner. This allowed for the calculation of average scores at a component level, module level and board level.

The first stage of data analysis was to perform a "Gage R&R" study on the generated data set to understand the acceptability of the developed cleaning efficiency metric. Gage R&R is a type form of measurements system quality analysis, were the measurement format is evaluated for its repeatability and reproducibility. The study illustrated in Section 5.2.4 and Appendix B,

provided the information regarding the accuracy of the cleaning score data. The calculated range of accuracy was used to readjust target cleaning scores by incorporating measurement variations.

The second stage of data analysis involved the calculation of aggregate average score of each round of experiment; the aggregate score was the average of the component underside average score and the component footprint average scores. To filter the data and increase accuracy, components which were always found to be clean were filtered out of the score when comparing across different cleaning techniques.

The third stage of data analysis was to analyze at the module and component level to look for trends in the data set. Trends and data comparisons would provide a tool to understand the contribution of each process parameters. The data set was analyzed to study the following effects on cleaning efficiency

- Effect of agitation
- Effect of cleaning solution
- Effect of time of cleaning process
- Effect of temperature of cleaning process
- Effect of product and component architecture

5.3.2 Criteria for Process Selection

Once the contribution of each process parameter to cleaning efficiency was understood, selection of the optimal cleaning process was undertaken. The main criterion for process selection was to maximize cleaning performance. The cleaning score was defined as a function of the four primary process parameters which were weighted by their impact on cleaning process. Therefore the process selection criteria were to maximize cleaning score through optimal combination of agitation, chemical concentration, time and temperature.

Analysis of experiment data would result in determining the states of the four process parameters which would provide efficient cleaning. The process parameter that would be deemed most important would be selected first followed by similar selections of lesser significant process parameters.

5.3.3 Methods to Optimize Cleaning Process

The selected cleaning process was optimized with an objective to attain highest process performance. Optimization was done by first selection the following two parameters

- The type of agitation: Ultrasonic, Centrifugal or Soak
- Type of cleaning solution: DI water, Chemical A or Chemical B.

This was done because both of these factors had significant associated costs. Once the best type of agitation was determined optimization would be more practical to be carried out on only that particular technique. The next step was to develop a 2^2 full factorial designed experiment with a center point with the two factors being the ones that can be altered in the selection combination of agitation and cleaning techniques.

After the optimization experiments were carried out DOE analysis tools such as ANOVA (analysis of variance) study, surface modeling and contour mapping were used to find the optimal values of the two varied factors to achieve maximum cleaning sore.

6. Results and Discussions

6.1 Analysis of Hypotheses Validation Experiments

In order to select the most suitable cleaning process, the results of the hypotheses validation experiments were analyzed. The analysis in this section was carried out to understand the effect of the four primary process parameters on the cleaning process.

6.1.1 Effect of Agitation on Cleaning Efficiency

In the validation experiments, boards were subjected to either a soak process before water wash or to ultrasonic agitation. A total of thirteen boards were subjected to soaking of which seven were soaked in a saponifier solution and the rest in plain DI water. Similarly, ten boards were subjected to ultrasonic agitation with five soaked in DI water and the other five exposed to ultrasonic agitation.

Table 6-1 Aggregate scores of ultrasonic agitation and soaking

Agitation	Cleaning Solution	Aggregate Average Score
Ultrasonic	7.5% Chemical A or B	4.9
Ultrasonic	DI Water	4.7
Soak	7.5% Chemical A	3.4
Soak	DI Water	1.6

Test results indicate that ultrasonic agitation produces much higher cleaning efficiency than a soak process. Table 6-1 illustrates that the average score of boards cleaned using ultrasonic agitation with DI water is 4.7 and the score is 4.9 if cleaned in saponifier solution. On the other hand, boards that were soaked in saponifier solution scored 3.4, whereas the ones soaked in DI water were nearly completely unclean with a score of 1.6. Ultrasonic cleaning's higher efficiency as compared to soak cleaning is illustrated in Figure 6-1, where both DI water and saponifier based experiments are compared. The trends in the data indicates that irrespective of cleaning times ultrasonic cleaning provides a much more effective medium for the cleaning solution to enter lower standoff components such as the 1210 Chip Capacitor and MLP FET .

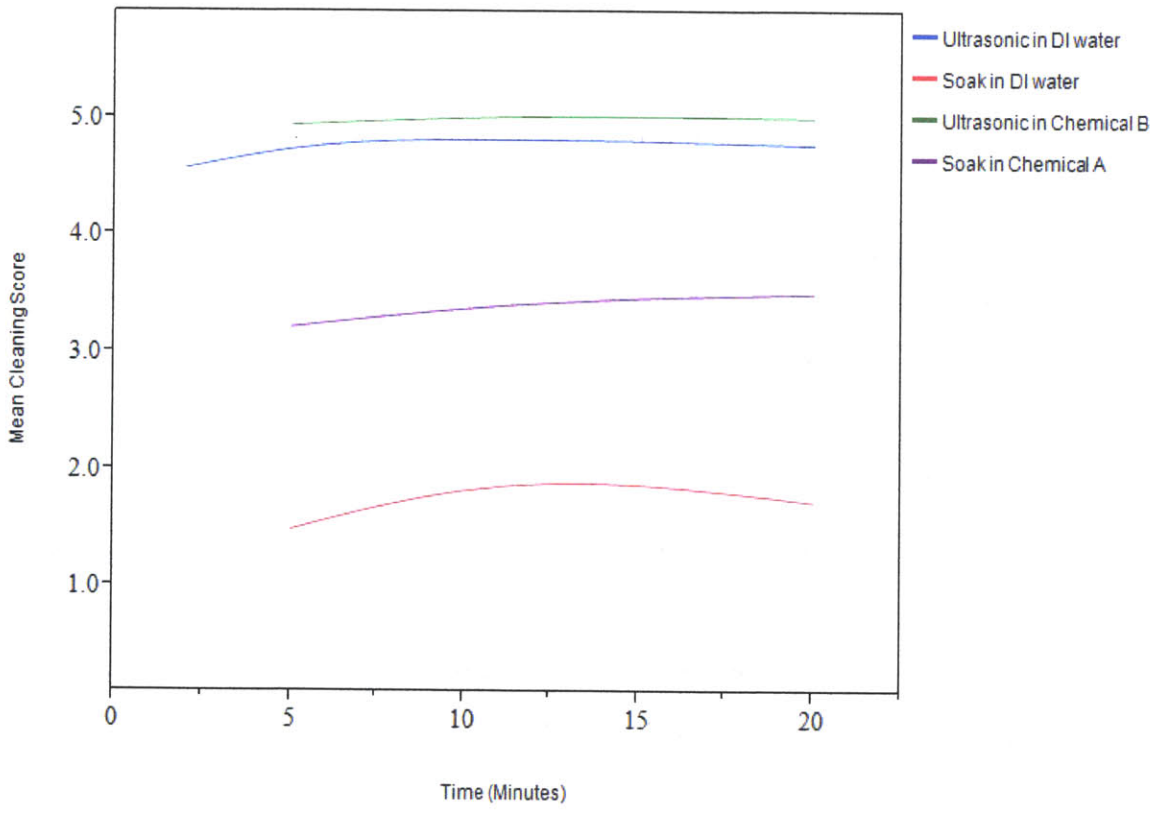


Figure 6-1Comparison of cleaning scores of ultrasonic and soak cleaning in DI water

6.1.2 Effect of Cleaning Agent Concentration on Cleaning Efficiency

Two types of saponifiers were used in the experimental study, they have been termed Chemical A and Chemical B. Both of these chemicals were used in the validation experiments to decrease the surface tension of the cleaning solution, thus enabling the solution to enter low standoff regions to dissolve solder flux residue and flush them out. As specified, the cleaning process used pure DI water as the cleaning solution without any alkaline saponifier; however as part of the validation experiment the current centrifugal water wash process was run using a cleaning solution of varied concentrations of Chemical B. This particular set of experiments was ideal to understand the effect of chemical solution on cleaning efficiency, as all the other three process parameter were kept constant with only the concentration of Chemical B varying from 5 % to 12.5% by volume.

As it can be seen from the graph illustrated in Figure 6-2 the cleaning score increase from around 3.5 to around 4.5 as concentration increase from 5% to 12.5%; furthermore, it is also seen that there is no significant difference between 7.5% and 10%. The graph plots the average cleaning scores of each of the eight 1210 Chip Capacitors, hence the estimate of aggregate accurately represents the process efficiency. Experiments were not carried out beyond 12.5% because of the cost associated [2] and due to observations that high concentrations were corroding the copper layers on the PCB board [1].

Thus it can be concluded that contribution of a saponifying cleaning solution to cleaning process efficiency is significant and it validates the argument the a saponifier reduces the surface tension of the cleaning solution allowing it to access low standoff regions (less than $50\mu m$), allowing water soluble flux residue to dissolve and then flushing the solute out.

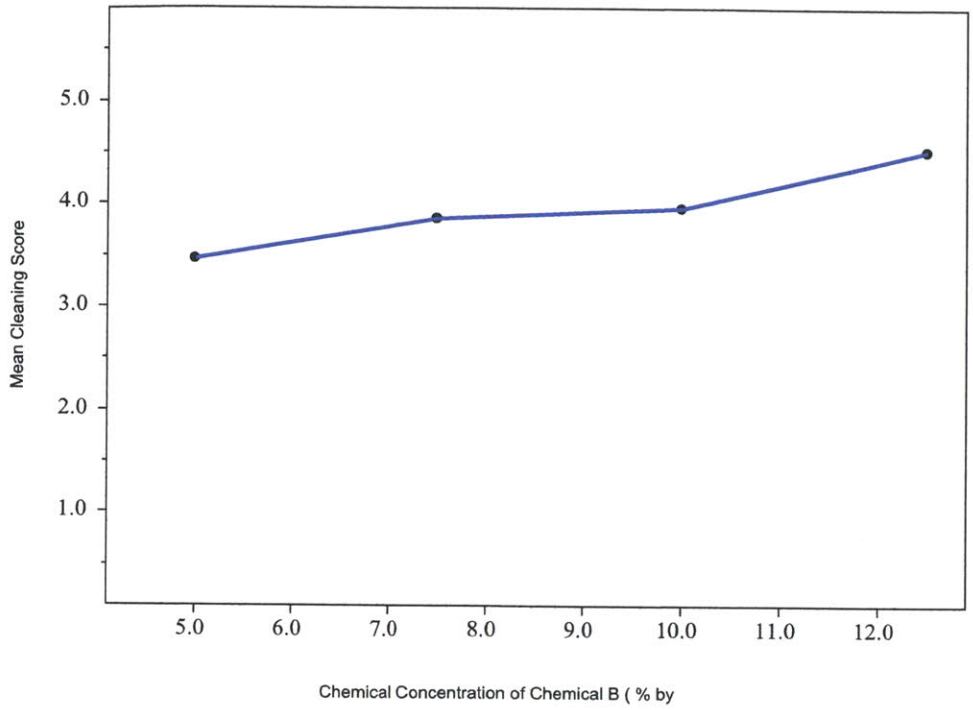


Figure 6-2 Comparison of cleaning scores of centrifugal cleaning with Chemical B

6.1.3 Effect of Time of Cleaning Process on Cleaning Efficiency

To understand the effect of cleaning process duration on cleaning efficiency, the PCB boards washed using ultrasonic agitation in DI water were studied. This particular cleaning technique was chosen as it is known that Ultrasonic agitation in DI water produced good cleaning results with average scores in the range of 4.5 to 5. A total of 5 experiments were carried out with process times of 2,5,10 and 20 minutes with replicates at 10 minutes, thus proving a large data set.

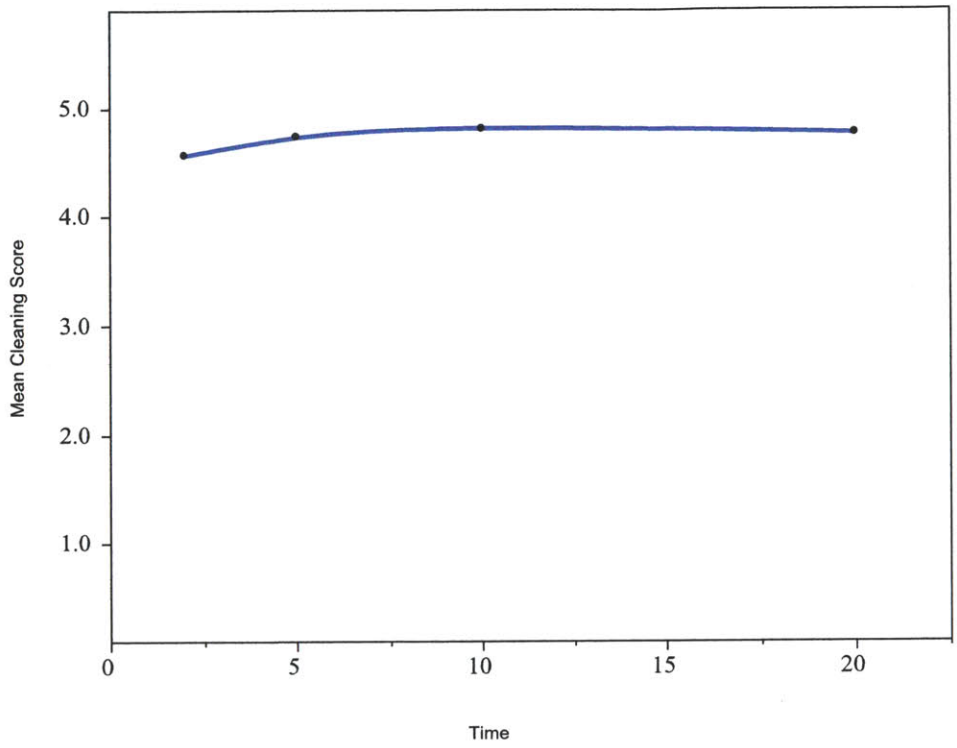


Figure 6-3 Comparison of cleaning scores of ultrasonic agitation in DI water

With temperature and agitation kept constant the cleaning scores vary only due to change in time of exposure. It can been seen in Figure 6-3 that the cleaning process efficiency increases steadily from 2 minutes to around 8 minutes where the curve tapers off until a cleaning time of 20 minutes. Therefore it can be concluded that time contributes to process efficiency but not to the degree of agitation and chemical concentration. Furthermore, it is concluded that the optimal process time for an ultrasonic cleaning process is in the range of 7 to 9 minutes.

6.1.4 Effect of Cleaning Solution Temperature on Cleaning Solution

In Chapter 4, it was found that process temperature does not affect cleaning process efficiency significantly in the relative temperature range of operation. Usual cleaning process is run at

operating temperatures in the range of 55^0C to 65^0C and study shows that cleaning efficiency is not sensitive to change in temperature in this range. One experiment with prewash soak cleaning in 7.5% Chemical A was carried out at 70^0C to attempt to validate the researched finding. The experiment results shown in Figure 6-4 agrees with the argument, it shows minimal change in process efficiency with a 10^0C change in temperature.

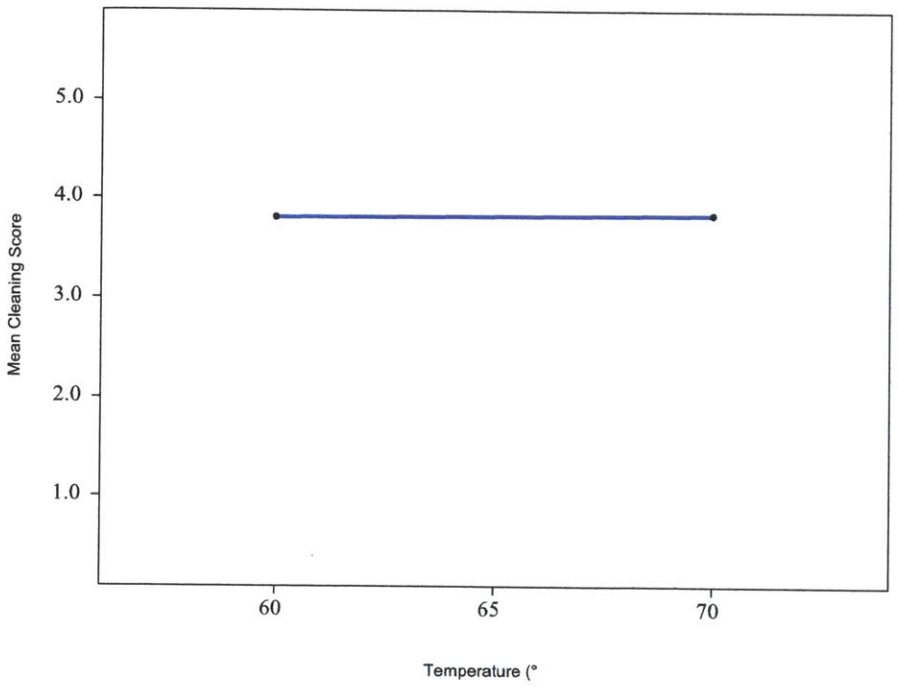


Figure 6-4 Comparison of cleaning scores of soak cleaning in 7.5% Chemical B

6.2 Design Factors Affecting Cleaning Efficiency

During the process of inspection, trends were observed between the same components located in different positions on the module and on the PCB board. This proved that the incidence of solder flux residue was dependent on:

- Position of component on a module
- Position of a module in a PCB board
- Architecture of power module

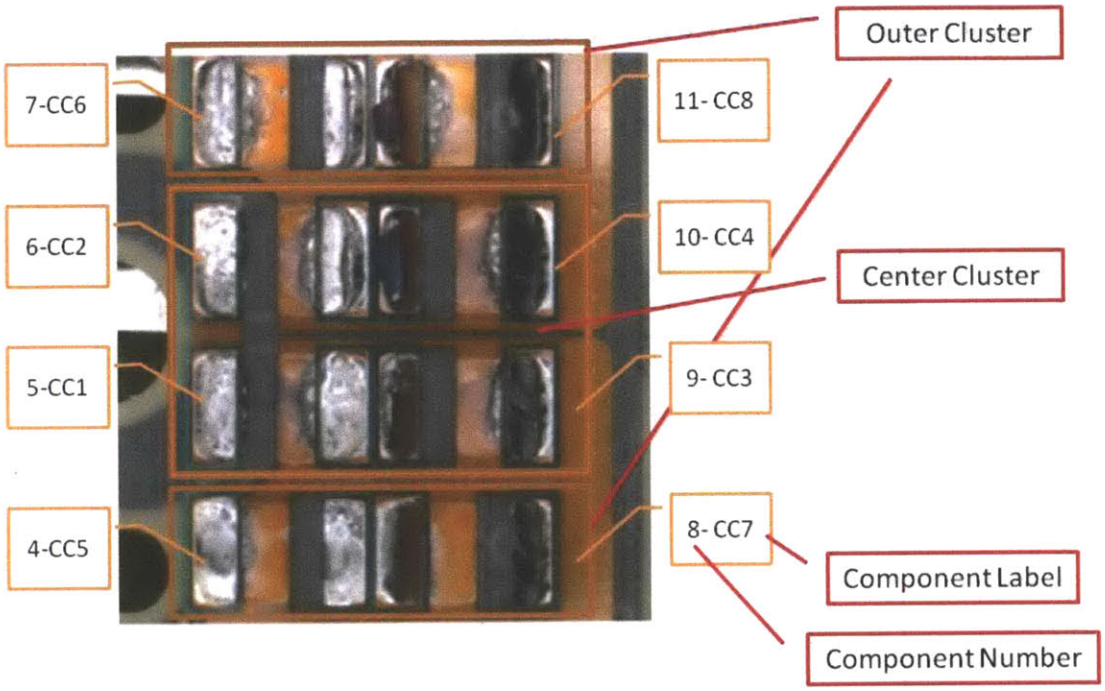


Figure 6-5 Footprint of bottom side 1210 chip capacitor array

To study the above three phenomena the 1210 chip capacitor array on the bottom side of the PCB board was analyzed. As show in Figure 6-5 this particular capacitor array consists of eight capacitors positioned in a 4 X 2 array. With eight capacitors per module and having critically low standoff heights of less than $50\mu m$, the 1210 capacitor proved ideal to study how cleaning efficiency varied in relation to position. The chip capacitors labeled CC1, CC2, CC3 and CC4 form the center cluster in the array and the one labeled CC5, CC6, CC7 and CC8 form the outer clusters. As illustrated in the Section 6.2., such a grouping was made as the center cluster was found to have larger amounts of flux residue than the outer cluster.

6.2.1 Effect of Component Location on Cleaning Efficiency

The eight sets of experiments carried out on the centrifugal water wash with chemical B gives the best scenario to study the effect of component location, this is because of the mode of agitation, time, temperature is highly standardized and they also have a large associated data set.

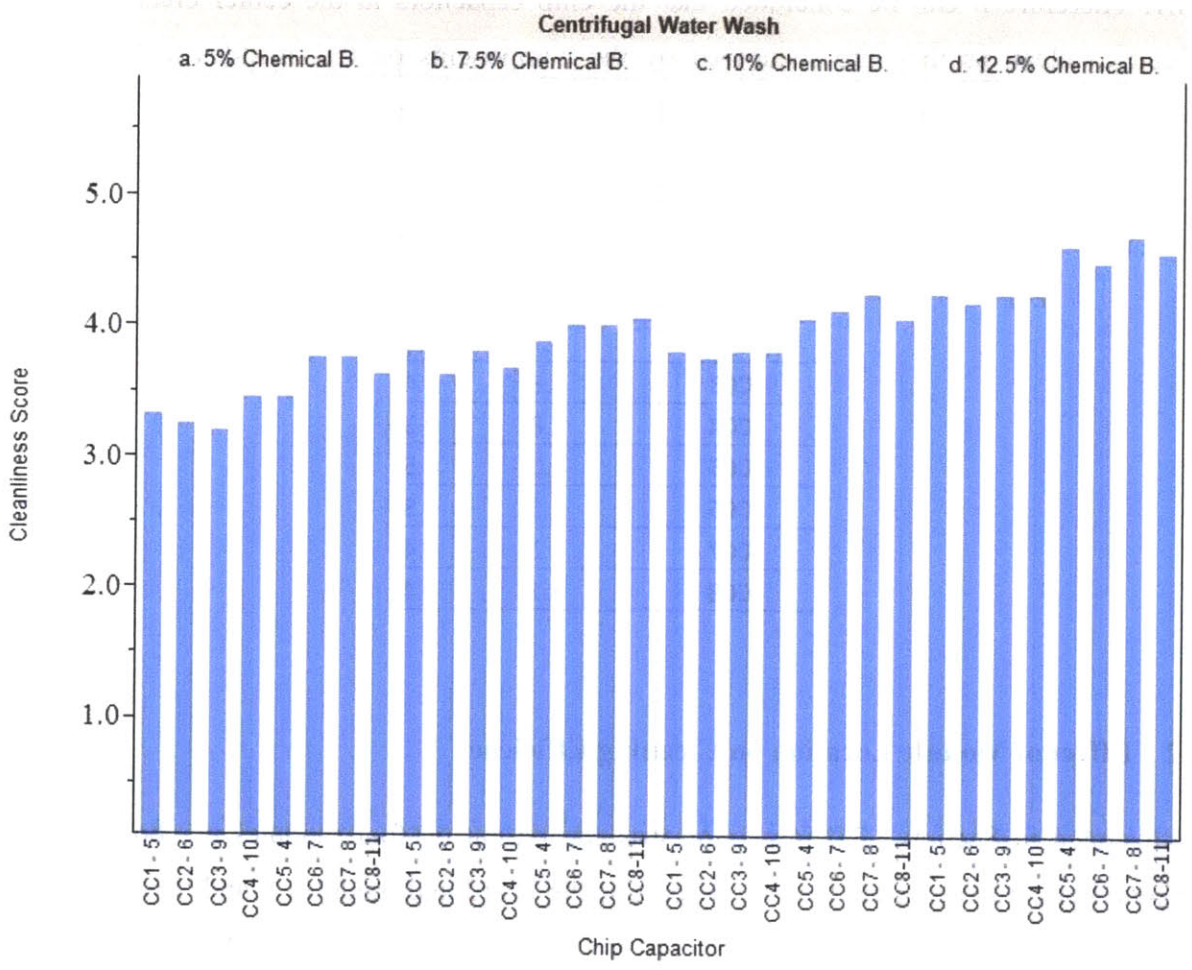


Figure 6-6 Variation of cleaning scores across capacitors in centrifugal water wash

Figure 6-6 illustrates the variation of cleaning scores across the eight 1210 capacitors in four different chemical concentrations. It can be seen that across all the four states the center cluster capacitors (CC1-CC4) have significantly lesser cleaning scores than the outer clusters (CC5-CC8). This is confirmed the results of the ANOVA study carried which shows that that the center cluster has a mean cleaning score of 3.8 while the outer cluster has a mean cleaning score of 4.1. Therefore it can be concluded that the chip capacitors in the center cluster are more difficult to clean as they are shadowed by the components on the outsides and centrifugal agitation is not sufficient to remove flux residue from these components.

Table 6-2 Mean and standard deviation of module cleaning scores

Component	Mean	Std Dev
CC1	3.8	0.4
CC2	3.7	0.4
CC3	3.8	0.4
CC4	3.8	0.3
CC5	4.0	0.5
CC6	4.1	0.3
CC7	4.2	0.4
CC8	4.1	0.4

6.2.2 Effect of Module Location on Cleaning Efficiency

As illustrated in Section 5.2.2 inspection was carried out on four modules per board, module numbers 4 and 13 were near the middle part of the board and modules 8 and 9 were on either side of the board.

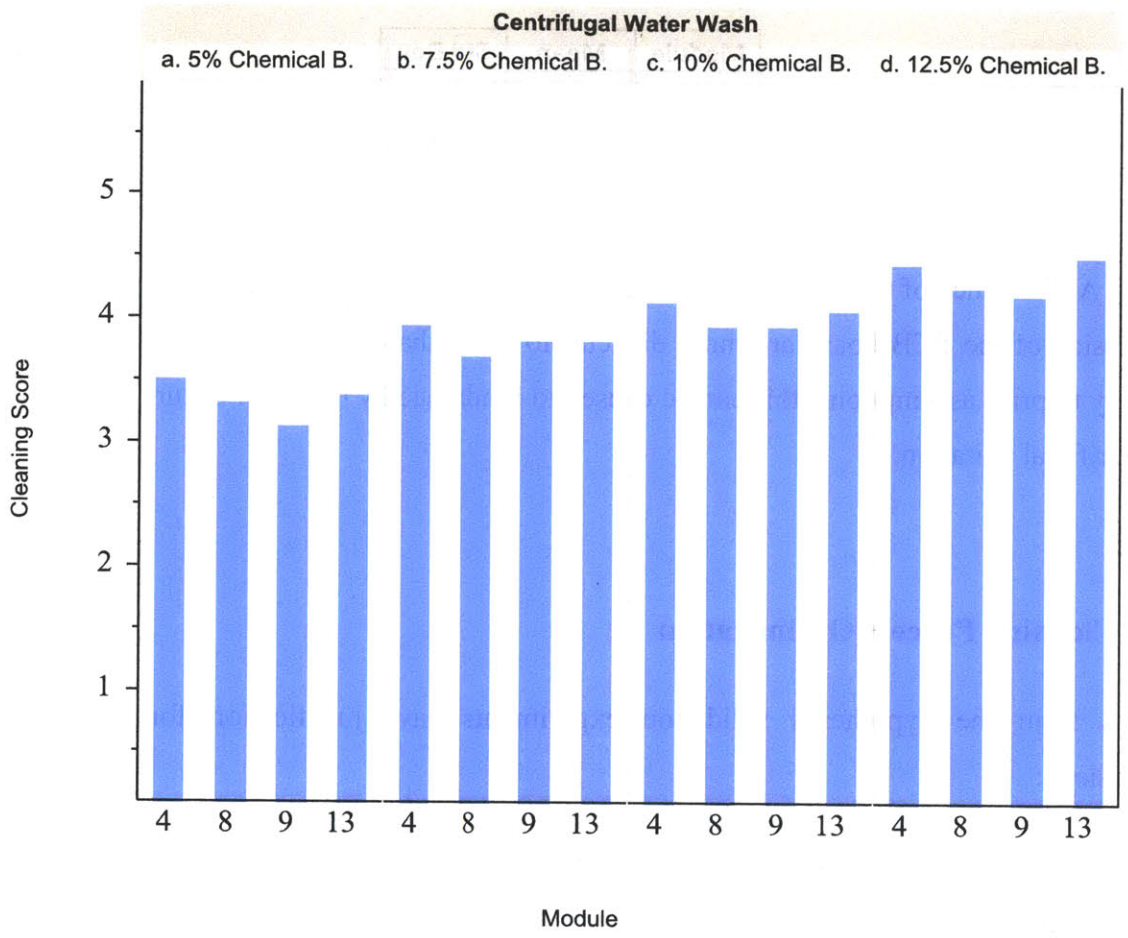


Figure 6-7 Variation of cleaning scores across modules in centrifugal water wash

As it can be seen in Figure 6-7, variations were observed across the four modules. The above graph represents the four sets of experiments carried out in the centrifugal water wash with varied concentrations of Chemical B. ANOVA analysis shows that Modules 8 and 9 have consistently produce lower scores than Modules 4 and 13.

Table 6-3 Mean and standard deviation of module cleaning scores

Module	Mean	Std Dev
4	4.0	0.4
8	3.8	0.47
9	3.8	0.4
13	4.0	0.4

A difference of 0.2 in cleaning score indicates that Modules 8 and 9 which are located on the outside of the PCB board are more difficult to clean than the ones in the inside. Although contrary to prior assumptions, this can be caused to hindrance by the wash fixture or inefficiency of centrifugal agitation.

6.3 Cleaning Process Optimization

Results from the hypotheses validation experiments gave justification for the following conclusions:

- Agitation has the most effect of cleaning process efficiency
- Characteristics of cleaning solution has next highest effect with saponifier such as Chemical B producing better results than DI water
- Time of wash process effects cleaning performance but its effect becomes negligible after 8 minutes.
- Temperature does not have significant effect in the relevant operational range of 60°C to 70°C

Using these conclusions the next step was to select the most suitable cleaning process followed by its optimization.

6.3.1 Optimal Cleaning Process Selection

The most suitable cleaning process was to be selected from the five cleaning techniques that were tested, which were:

- Ultrasonic agitation with saponifier as cleaning solution followed by rinse cycle.
- Ultrasonic agitation with DI water as cleaning solution followed by rinse cycle
- Centrifugal agitation water-wash with saponifier as cleaning solution.
- Prewash soak in saponifier followed by rinse cycle
- Prewash soak in DI water followed by rinse.

Agitation being the most important process parameter was also critical in terms of manufacturing system efficiency [2]. The three agitation choices were ultrasonic, centrifugal and prewash soak. As explained in Section 6.1, ultrasonic agitation performed much better than prewash soak and also better than centrifugal wash. In concurrence with the explanation in Section 6.1, in all the three agitation methods scores improved with changed over from DI water to a saponifier based cleaning solution. Ultrasonic agitation consistently achieved scores of higher that 4.8 in both DI water and saponifier based cleaning solution. The highest score achieved by any single centrifugal wash test was 4.5 and that by prewash soak was 3.8; therefore it can be convincingly argued that ultrasonic agitation removed solder flux residue better than centrifugal agitation or a prewash soak. Figure 6-8 illustrates the significant difference in cleaning efficiency across the three forms of agitation. The underside of the MLP-FET contains minimal flux residue in case of ultrasonic agitation while the other two perform much worse.

With ultrasonic selected as the best type of agitation the next step involved selecting between DI water based cleaning solution and a saponifier based cleaning solution. Figure 6-9, illustrated the inspection results for three different types of cleaning solutions. The chip-capacitor footprint contains a large amount of residue in case of DI water, flux residue decrease when a saponifier based solution is used. In all experiments carried out, it was observed that high standoff regions

were cleaned by DI water and saponifier based solutions but low standoff regions were cleaned only by saponifiers. Furthermore, the selection of Chemical B over Chemical A has been explained by Jain [1] were he shows how Chemical A etched the copper layers on the PCB board.

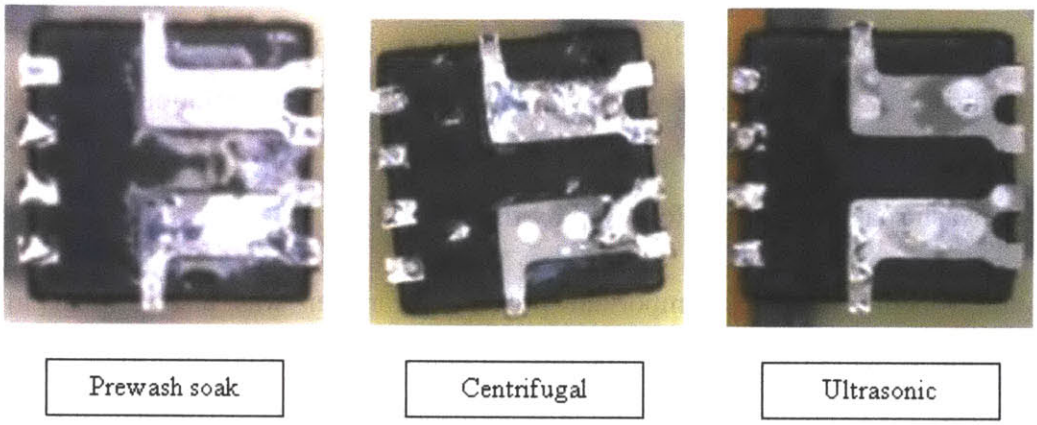


Figure 6-8 MLP-FET underside: Variation across three agitations techniques in DI water

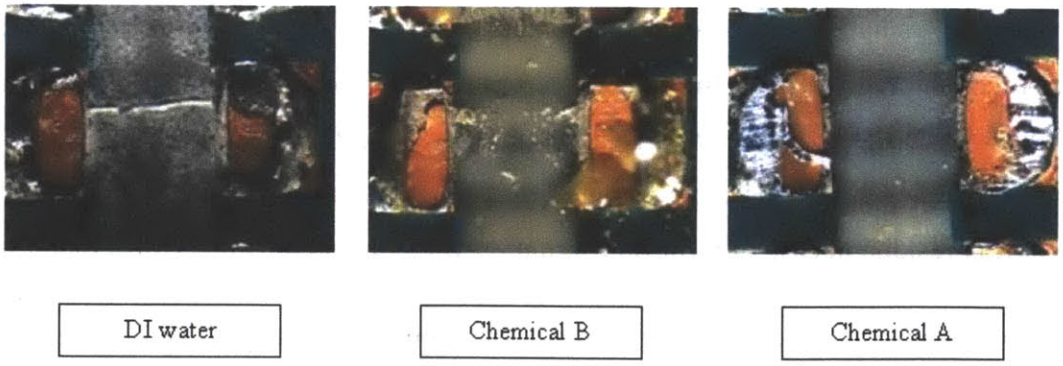


Figure 6-9 Chip-Capacitor footprint: Prewash soak in three chemical solutions for 10 minutes

The effect of time as explained in Section 6.1.3 was found to be significant up to around 10 minutes after which cleaning performance stayed the same. Temperature on the other hand

produced very little effect on any of the experiments carried out. Therefore, it can be concluded that of the five different techniques ultrasonic agitation with Chemical B cleaning solution produced very high rates of cleaning as compared to the other four techniques.

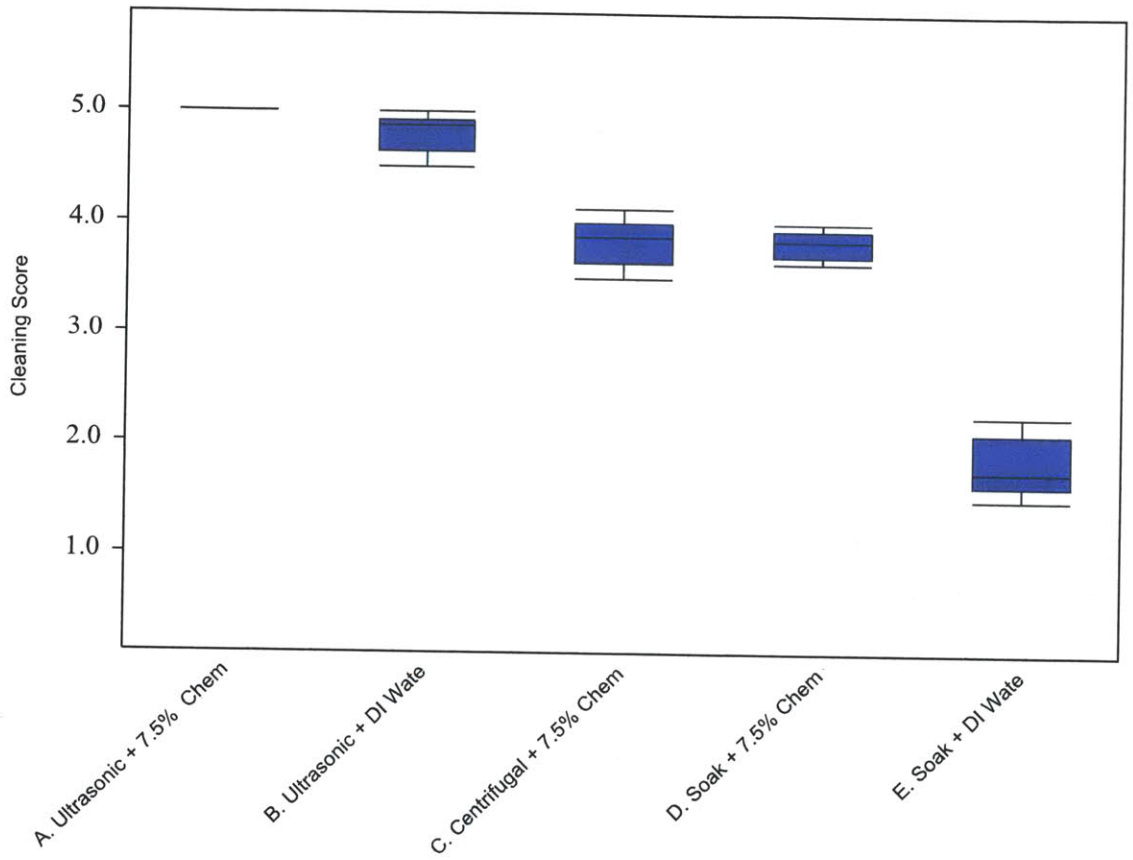


Figure 6-10 Comparison of cleaning techniques

The Figure 6-10 helps understand the difference in cleaning performance of the five techniques across the entire experiment data set. From the box plots of observations, it can be seen that the saponifier experiments taken at 7.5% concentration of chemical B with ultrasonic agitation consistently produces cleaning scores of 5, while with DI water produces an average

cleaning score of 4.8. Centrifugal agitation and prewash soaking with Chemical B produce similar results, while prewash soaking in DI water leaves components nearly unclean. Table 6-3 shows the difference in process performance across the five techniques.

Table 6-3 Experiment results of five cleaning techniques

Agitation	Cleaning Solution	Time (min.)	Temperature (°C)	Component Average Score	Footprint Average Score
Ultrasonic	7.5% Chemical B	10	60	5.00	5.00
Ultrasonic	DI Water	10	60	4.86	4.83
Centrifugal	7.5% Chemical B	20	60	3.81	3.86
Soak	7.5% Chemical B	10	60	3.61	4.00
Soak	DI Water	10	60	1.61	2.08

As it was explained in Section 5.3.2 the criteria for process selection was to achieve the maximum cleaning score of 5. Prewash soak in DI water was only 37% efficient with an average score of 1.85 out of a maximum of 5. Centrifugal wash and prewash soak in Chemical B were 76% efficient, attaining scores of around 3.8. On the other hand ultrasonic agitation produced near perfect scores of above 4.9. Furthermore, ultrasonic agitation in 7.5% Chemical B solution achieved absolute cleaning in all experiments. Therefore from the comparison of the different cleaning techniques it can be concluded that cleaning with ultrasonic agitation and Chemical B cleaning solution is the best cleaning technique.

6.3.2 Design of Experiment for Process Optimization

From Section 6.3.1, ultrasonic agitation and Chemical B were selected as two of the four process parameters. As explained in Section 6.1.4 the temperature of cleaning process was not a significant factor so the used temperature of 60°C was deemed suitable. However, it was known that time of cleaning process has an effect on the process performance so it formed one of the

parameters to be optimized. With agitation and time selected, the concentration of Chemical B was the other parameter that could be varied.

As a result, the objective of process optimization was to produce an optimal combination of chemical concentration and time, while still achieving the maximum cleaning performance. A reduction in both of these factors will result in increases manufacturing system efficiency as explained by Rajendran [2].

In order to find the optimal combination of time and temperature a 2^2 factorial experiment has been designed with an additional experiment to calculate the center point. The two levels of time were taken as 4 minutes and 10 minutes, as it was see that the effect of time is prominent up to about 8 minutes after which it stagnates. The two levels of concentration were taken as 2.5% and 7.5%, as it was known that 7.5% concentration produced cleaning scores of 5 consistently. To provide more accuracy and capacity to plot the response, a center point was taken at 5% concentration and 7 minutes duration.

Table 6-4 DOE for cleaning process optimization

Cleaning Process Optimization				
S. No.	**Agitation**	**Cleaning Solution (% conc. per volume)**	**Time (min)**	**Temp (°C)**
1	Ultrasonic	2.5% Kyzen	4	60
2	Ultrasonic	2.5% Kyzen	10	60
3	Ultrasonic	5% Kyzen	7	60
4	Ultrasonic	7.5% Kyzen	4	60
5	Ultrasonic	7.5% Kyzen	10	60

6.3.3 Result of Process Optimization

Optimization experiments were carried out with an objective of achieving the maximum cleaning score of five. As explained in Section 5.3, a "Gage R&R" study was carried out to estimate the accuracy of the grading metric. The results of the study (Appendix C) indicated that inspector error is minimal; hence the objective cleaning score remained as five. Like in the case of Section 6.1 and 6.2, the analysis of the five sets of optimization experiments was done based on the 1210 chip capacitor array and the MLP-FET.

Experimental results indicate the cleaning scores gradually increase with increase in time and increase in chemical concentration. Absolute cleaning is achieved at the center point and at 7.5% concentration and 10 minutes. In contrast to the results in Section 6.1, the effect of time was observed to be larger than the effect of concentration. This is due to the fact that 2 minutes is a very short time for even ultrasonic agitation to clean and cleaning gradually improves up to the center point and then stagnates. It is also evident the accuracy of the optimization process would be increased with more data point at more factor level. The contour map in Figure 6-12 illustrates this shortcoming as the lower right corner shows slightly lesser cleaning scores due to its distance from the center point. However, this can be attributed to having only two factor levels.

The experiment results are illustrated in the surface plot in Figure 6-11; it shows that at 2.5% Chemical B and 4 minutes a produces a cleaning score of 4.8. As the chemical concentration is increase to 7.5% the score increases to 4.8 and an increase in time to 10 minutes increases the score to 4.9. The peak in the surface plot at the center and the top right corner indicate that the maximum cleaning score of 5 is achieved along the line connecting these two points.

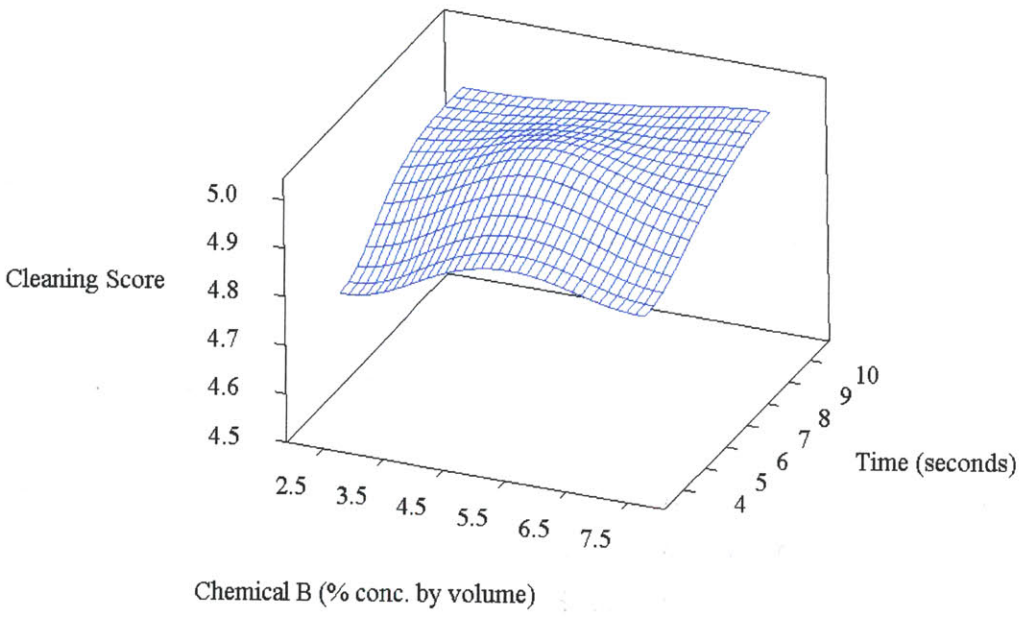


Figure 6-11 Surface plot of cleaning score vs. time and Chemical B concentration

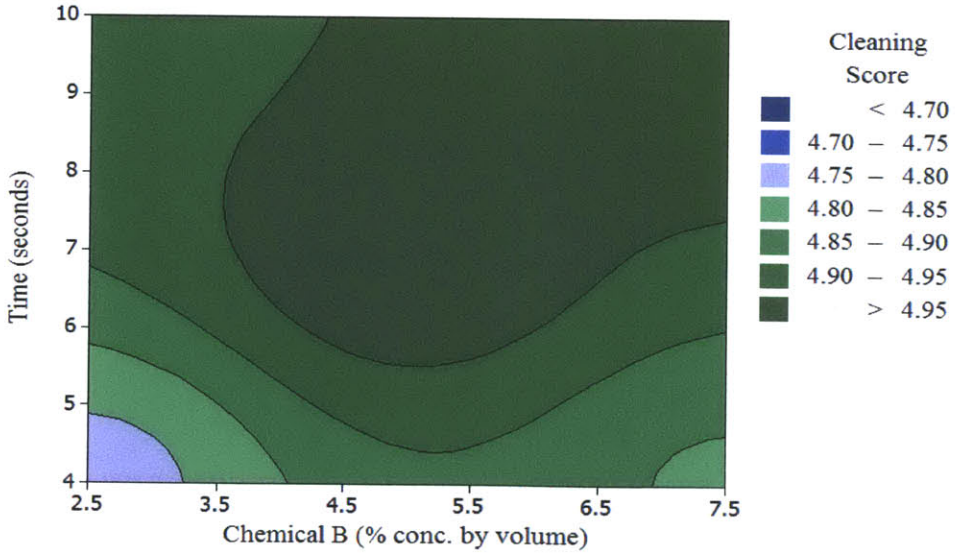


Figure 6-12 Contour plot of cleaning score vs. time and Chemical B concentration

The contour map in Figure 6-12 sheds light on the region of optimum process performance. As it can be seen a cleaning score of more than 4.95 can be achieved in the region around the center point with concentration as low as 3.5% and time as low as 5.5 minutes. Rajendran [2] in his work explains how chemical concentration is much more significant than time with regards to production cost. Wash times below 20 minutes do not affect the production cycle time so in this case minimization of chemical concentration is taken as the chief objective.

Therefore to attain cleaning score of 5 the center point of 5% chemical concentration and 7 minutes were the optimal values. The maximum cleaning score can be achieved if process is operated at any values on the line connecting these optimal values and the extreme value of 7.5% and 10 minutes. Furthermore upon optimization, it is seen that a cleaning score greater than 4.95 can be achieved if process is operated in the dark green region of the contour map shown in Figure 6-12. This would be helpful during implementation of control standards during process implementation.

7. Summary, Recommendation and Future Work

7.1 Summary of Cleaning Process Selection and Optimization

The validation experiments of the hypotheses formulated in [2] was carried out on a pre-wash test cycle; this station was placed between the visual inspection station and the centrifugal water wash process in the manufacturing facility. The main objective of hypotheses validation experiments was to identify and understand the primary process parameter that determined efficient cleaning of power modules. A visual inspection based cleaning efficiency metric was developed to quantify the efficiency of a cleaning process. Component specific metric were also developed for greater accuracy and a gage R&R study was carried out for the measurement system. The hypotheses validation experiments yielded the following results:

- Type of agitation in the most significant factor that determines efficient cleaning and ultrasonic agitation gave the best results
- A saponifier based cleaning solution removed solder flux residue better than DI water.
- An increase in wash time up to 8 minutes improved cleaning, but cleaning performance remained constant for longer periods.
- Variation in temperature in the 60°C-70°C range did not significantly affect cleaning.
- Components surrounded by other components were harder to clean.

- Modules positioned in the middle of the PCB board were cleaned better than the module on either end of the PCB board.

These resulted in the selection of ultrasonic cleaning with chemical B solution as the optimal cleaning technique. The selected technique was optimized for chemical concentration and wash time using a 2^2 factorial DOE. Experimentation and ensuing inspection revealed that to achieve a cleaning score of more than 4.95, a chemical B concentration of 3.6% and wash time of 7.7 minutes was required. The experiment center point of 5% concentration and 7 minutes wash time achieved the cleaning score of 5. Therefore, it can be concluded that given the current product architecture an optimized chemical B based ultrasonic cleaning technique achieves absolute cleaning efficiency. Furthermore, in the case of changes in product architecture there is scope for the application of ultrasonic cleaning without a saponifier.

7.2 Recommendation

The following recommendations are offered regarding the cleaning process in SMT assembly line of the manufacturing facility:

- The company should change the current DI water wash cleaning system with a batch-type ultrasonic cleaning system. The wash cycle should be carried out in a 5% Chemical B solution at 60°C for 7 minutes. This is to be followed by a DI water based rinse cycle. Furthermore, the current centrifugal system has no scope to be further optimized to improve the magnitude of agitation.
- The company should revaluate product architecture to improve cleaning by developing new design for manufacturing rules. Low standoff components such as chip capacitors and MLP-FET should not in the shadow of larger components or over copper pads. If

these design rules are implemented DI water based ultrasonic cleaning would remove flux residue

- The use of saponifier based cleaning solution improves cleaning efficiency by allowing water to enter low standoff regions. The solder flux residue is water soluble and can be removed by DI water.

7.3 Future work

7.3.1 Implementation of Ultrasonic Cleaning Method

The current DI water based centrifugal washing system is unable to remove solder flux residue from low standoff regions. To reduce product failure rates and improve production quality an ultrasonic cleaning system should be installed in place of the centrifugal cleaning system. The new system will need to be qualified and installed. New process control techniques will have to be installed as current omega meter is not sufficient to detect flux residue. If a saponifier based cleaning system is used installation would have to go through infrastructure, purchase and environmental regulations.

7.3.2 Component and Product Architecture Changes

This research revealed that there is scope for improvement in both module design and component design. Critical components such as MLP-FET's can be replaced by similar components with single leads and less complex through channels. Simpler footprint deign would allow development of flow channels during cleaning. Similarly all such critical components should be reviewed to enable better manufacturability. In terms of module design, there is scope for development of design for manufacturing (DFM) rules; this would help prevent avoidable product failures.

Appendix A: Run chart of experiments

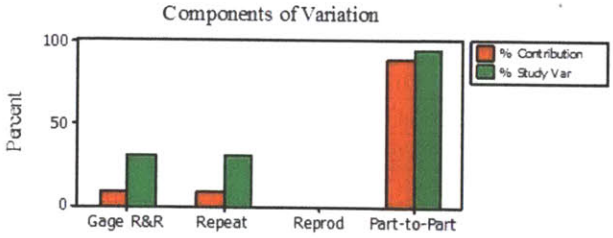
	S. No.	Board #	Agitation	Chemical Conc. (v/v)	Time (min)	Temp (^{0}C)
Experiment 1 Hypothesis - Testing	1	35	Twice water washed	DI Water	10	60-65
	2	36	Twice water washed	DI Water	10	60-65
	3	40	Soak	DI Water	5	60
	4	41	Soak	DI Water	10	60
	5	42	Soak	DI Water	20	60
	6	43	Soak	7.5% Chemical A	5	60
	7	44	Soak	7.5% Chemical A	10	60
	8	45	Soak	7.5% Chemical A	20	60
	9	46	Soak	7.5% Chemical B	10	60
	10	47	Ultrasonic	7.5% Chemical B	5	60
	11	48	Soak	DI Water	60	60
	12	52	Ultrasonic	DI Water	5	60
	13	53	Ultrasonic	DI Water	10	60
	14	54	Ultrasonic	7.5% Chemical A	5	60
	15	55	Ultrasonic	7.5% Chemical A	10	60
	16	56	No water wash	n/a	n/a	n/a
	17	57	Soak	DI Water	40	60
	18	58	Soak	DI Water	60	60

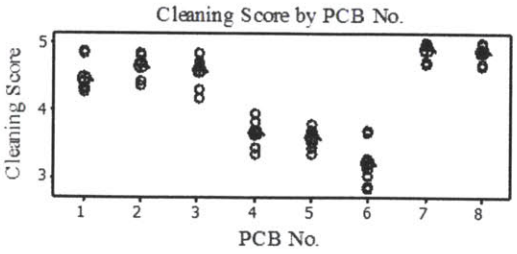
	S. No.	Board #	Agitation	Chemical Conc. (v/v)	Time (min)	Temp (^{0}C)
Experiment 2 Current Process Optimization & Repeatability Test	19	396	Centrifugal	7.5% Chemical B	20	60
	20	397	Centrifugal	7.5% Chemical B	20	60
	21	399	Centrifugal	10% Chemical B	20	60
	22	400	Centrifugal	10% Chemical B	20	60
	23	401	Centrifugal	12.5% Chemical B	20	60
	24	402	Centrifugal	12.5% Chemical B	20	60
	25	403	Centrifugal	5% Chemical B	20	60
	26	404	Centrifugal	5% Chemical B	20	60
	27	405	Ultrasonic	DI Water	2	60
	28	406	Ultrasonic	DI Water	10	60
	29	407	Ultrasonic	DI Water	20	60
	30	409	Soak	7.5% Chemical B	10	60
	31	410	Soak	7.5% Chemical B	10	70
	32	411	Soak	7.5% Chemical A	10	60
	33	412	Ultrasonic	7.5% Chemical B	5	60

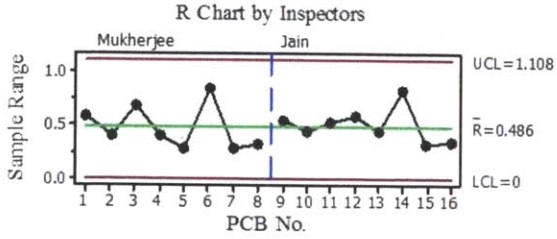
	34	413	Ultrasonic	7.5% Chemical A	5	60
Experiment 3 Alternate MLP-FET Test	35	680	Water Wash		20	60
	36	681	Ultrasonic	DI Water	5	60
	37	682	Soak	7.5% Chemical B	10	60
	38	683	Ultrasonic	7.5% Chemical B	5	60
Experiment 4 Process Optimization	38	858	Ultrasonic	2.5% Chemical B	4	60
	39	859	Ultrasonic	2.5% Chemical B	10	60
	40	860	Ultrasonic	5% Chemical B	7	60
	41	861	Ultrasonic	7.5% Chemical B	4	60
	42	862	Ultrasonic	7.5% Chemical B	10	60
	43	863	Ultrasonic w/o rinse	DI Water	10	60

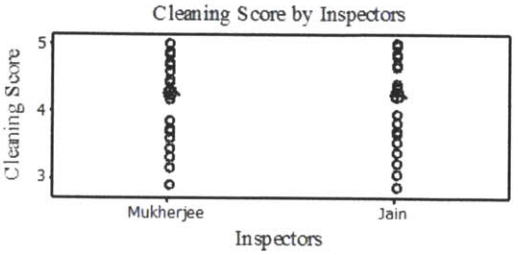
Appendix B: Summary of Gage Repeatability and Reproducibility Study (R&R)

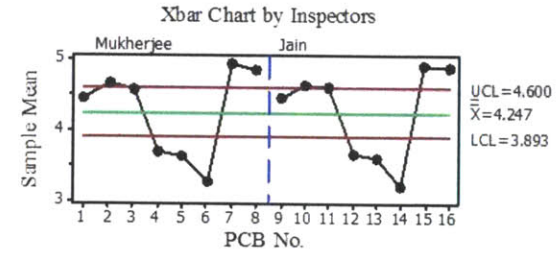
Gage R&R Study - ANOVA Method					
Two-Way ANOVA Table With Interaction					
Source	DF	SS	MS	F	P
Moduels	7.00	23.97	3.42	1750.03	0.00
Inspectors	1.00	0.00	0.00	1.10	0.33
Modules * Inspectors	7.00	0.01	0.00	0.04	1.00
Repeatability	48.00	2.43	0.05		
Total	63.00	26.42			
Alpha to remove interaction term = 0.25					
Two-Way ANOVA Table Without Interaction					
Source	DF	SS	MS	F	P
Moduels	7.00	23.97	3.42	76.97	0.00
Inspectors	1.00	0.00	0.00	0.05	0.83
Repeatability	55.00	2.45	0.04		
Total	63.00	26.42			

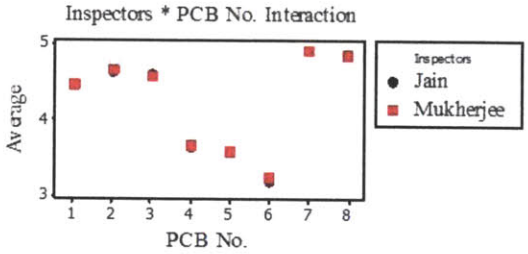

Components of Variation
Percent
100
50
0
% Contribution
% Study Var
Gage R&R
Repeat
Reprod
Part-to-Part


Cleaning Score by PCB No.
Cleaning Score
5
4
3
1 2 3 4 5 6 7 8
PCB No.


R Chart by Inspectors
Mukherjee
Jain
Sample Range
1.0
0.5
0.0
UCL=1.108
R̄=0.486
LCL=0
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
PCB No.

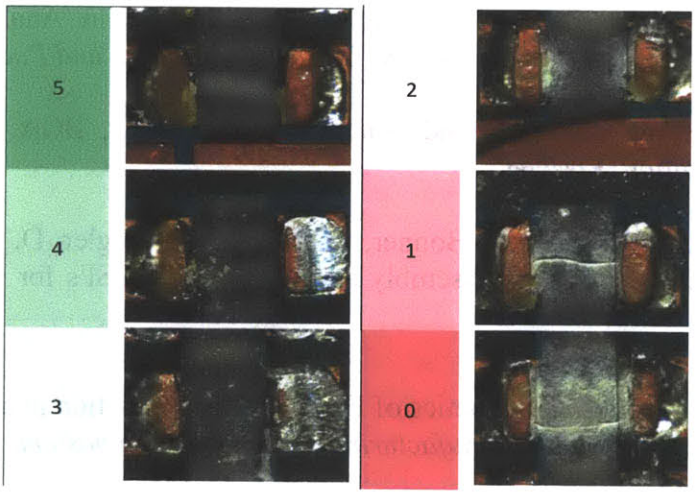

Cleaning Score by Inspectors
Cleaning Score
5
4
3
Mukherjee
Jain
Inspectors


Xbar Chart by Inspectors
Mukherjee
Jain
Sample Mean
5
4
3
UCL=4.600
X̿=4.247
LCL=3.893
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
PCB No.


Inspectors * PCB No. Interaction
Average
5
4
3
Inspectors
Jain
Mukherjee
1 2 3 4 5 6 7 8
PCB No.

Appendix C: Component Footprint Grading Scale

Cleaning Performance Metric	
Score	**Description**
5	Completely Clean
4	Trace - Minute Amounts
3	Low flux residue incidence
2	Non-Uniform residue presence
1	Uniform residue presence
0	Large amounts of residue



Footprint Scoring Methodology: 0603 Chip Capacitors

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